Si Nanoelectronic Device Technology

IEEE EDS WIMNACT 23

@North-Eastern Hill University, Shillong

April 5, 2010

Tokyo Institute of Technology

Frontier Research Center

Hiroshi Iwai

Tokyo Institute of Technology

Founded in 1881, Promoted to Univ. 1929

Institute Overview

Einstein Visit

Established in 1881→ 130th anniversary in 2011

3 undergraduate schools

School of Science, School of Engineering, School of Bioscience and Biotechnology

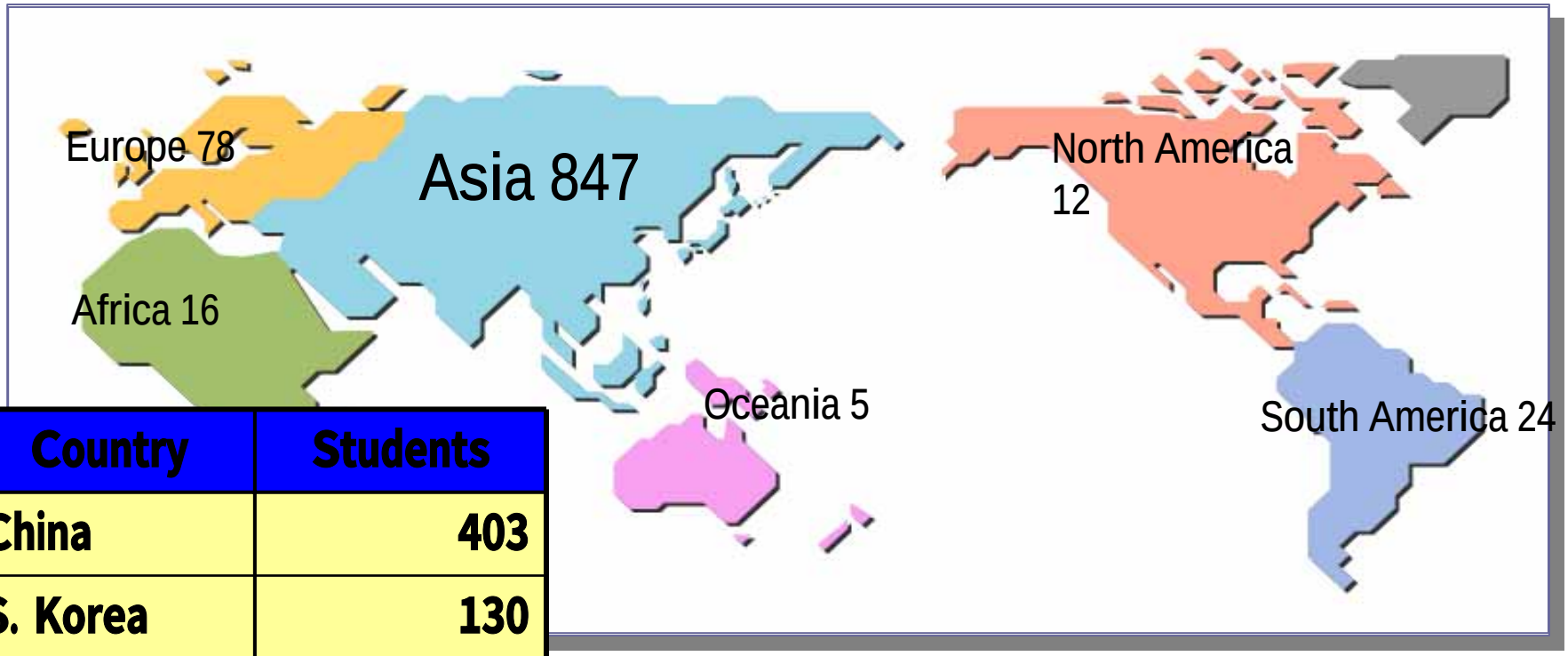
7 graduate schools

Science and Engineering Science, Science and Engineering Technology,
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

	Undergraduate	Graduate	Master's	Doctoral	Teaching Staff	Student/Instructor	Staff
Tokyo Inst.	5,000	5,000	3,500	1,500	1,200	8.3	550
Per Year	1,200		1,800	500			

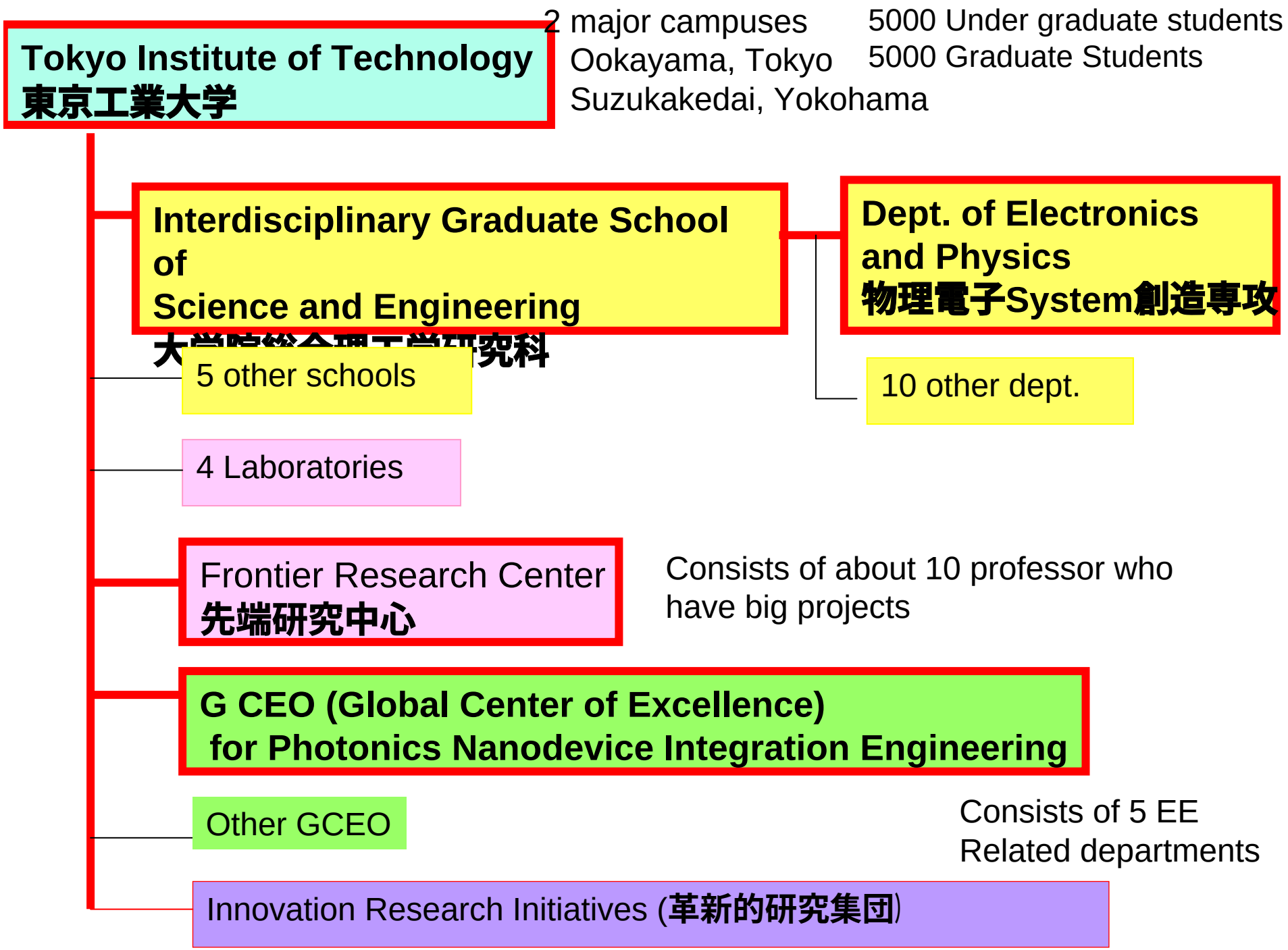
International Students



Country	Students
China	403
S. Korea	130
Indonesia	64
Thailand	55
Vietnam	60
Malaysia	28

Total 982

(As of May. 1, 2005)


Tokyo Institute of Technology
東京工業大学
2 major campuses
Ookayama, Tokyo
Suzukakedai, Yokohama
5000 Under graduate students
5000 Graduate Students
Interdisciplinary Graduate School of
Science and Engineering
大学院総合理工学研究科
Dept. of Electronics and Physics
物理電子System創造専攻
10 other dept.
5 other schools
4 Laboratories
Frontier Research Center
先端研究中心
Consists of about 10 professor who have big projects
G CEO (Global Center of Excellence)
for Photonics Nanodevice Integration Engineering
Other GCEO
Consists of 5 EE Related departments
Innovation Research Initiatives (革新的研究集団)

岩井研メンバー

（2009年11月1日現在）

教授
岩井洋

准教授（共同研究）
筒井一生

客員教授
Simon Min Sze

客員教授
服部健雄

特任教授
名取研二

連携教授
杉井信之

連携教授
西山彰

特任准教授
Parhat Ahmet

助教
角嶋邦之

博士研究員

Milan Kumar Bera

博士課程

D3
佐々木雄一朗

D3
下村浩

D3
宋在烈

D3
館喜一

D2
川那子高暢

D2
佐藤創志

D2
冨田隆治

D2
Maimaitirexiati Maimaiti

D2
Abudukeilmu Abudureheman

D1
幸田みゆき

D1
李映勲

籠井研 D3
小林勇介

修士課程

M2
新井英朗

M2
中山寛人

M2
船水清永

M2
細田亘

M2
又野克哉

M2
ﾀﾘｳｽ･ﾊｻﾝｻﾞﾃﾞ

M2
Mokhammad Sholihul Hadi

M1
小柳友常

M1
小澤健児

M1
神田高志

M1
澤田剛伸

M1
茂森直登

M1
向井弘樹

M1
呉研

M1
Dou Chunmeng

学部

籠井研 M2
横田知之

籠井研 M2
星野憲文

籠井研 M1
田中正興

B4
来山大祐

研究生

Rena Salmalti

スタッフ

松本昭子

辛川美琴

西澤　正子

Interdisciplinary Graduate School of Science and Engineering

大学院総合理工学研究科

J2 Building:

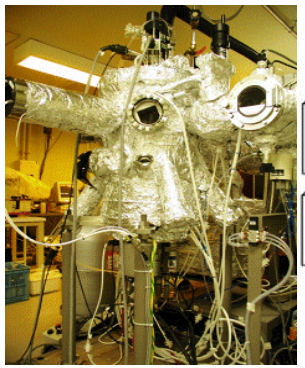
Frontier Collaborative Research Center（FCRC）
先端創造共同研究中心

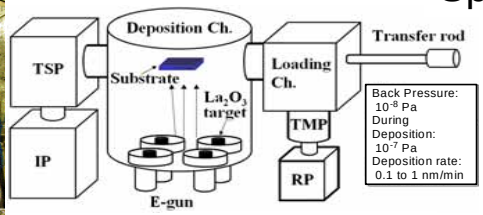
Iwai Lab. Equipment

MBE and Sputter Chamber

Sputter Chamber

1/f noise measurement system; 6 inch wafer





MBE Chamber

RTA Furnace No.1

RTA Furnace No.2

RF measurement system; 8 inch wafer, 40 GHz

岩井研究室 ~Iwai Lab.~

ご挨拶

Welcome to Iwai Lab.

総合理工学研究科　物理電子システム創造専攻　岩井研究室

当研究室では、シリコンをベースとした集積回路のデバイス技術、特に素子超微細化や集積回路限界の探査、研究や、新材料や三次元トランジスタ構造のシリコン集積回路への導入を行っています。さらにエマージング技術としてゲルマニウムやⅢ-Ⅴ族半導体チャネル材料の検討などを行っています。

LSI(Large scale integrated Circuit,大規模集積回路)の最初の製品とみなされるIntelの1k bit DRAMが製造されてから30年近くになりますが、この間にLSIは実に長足の発展を遂げ、高度な計算を行い動作や情報を制御する中枢部品としてありとあらゆる機器に用いられるようになってきました。

最近のMobile Telephone, Mobile PC, ひいてはインターネットの爆発的な普及も軽量、小型、低消費電力で極めてきたことによるものです。

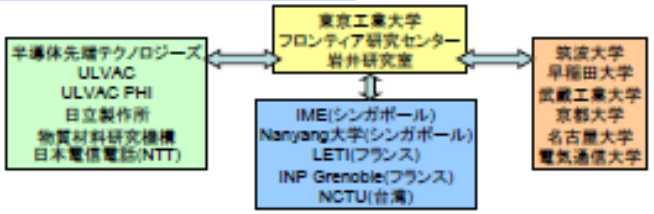
今後更にこの文明飛躍的な発展を遂げて、近い将来人間の知性、感性の機能を代行する機器が出現することが大いに期待されます。

これはこれからの高齢化社会で予想される労働人口不足、老人介護人口不足などの状況のもとで、各人が平等にある程度以上の生活レベルを教授できるためには行く行くは超えなければならないハードルであると考えますが、何れにせよこれを実現するためには現状のものから何桁も性能の高い機器の実現が必要であると考えられており、まずはハードとしてのLSIの発展が今後何十年かにわたって継続していくことが必要条件のひとつとも考えられています。

さて、LSIの発展はトランジスタを中心としたLSI中の素子の縮小化によってなされてきましたが、トランジスタの縮小化の限界がどこにあるかが重要な疑問としてクローズアップされてきます。この流れが今後も続くとすると2005年頃にはゲート長が30nmとなり、更に今世紀の半ばにはゲート長はシリコン結晶中の原子の間隔である0.0003μm(即ち3Å)となる計算となります。この寸法辺りが原子を用いてトランジスタを形成する限りにおいて究極的な限界と考えられますが、このようなゲート長のトランジスタが動作するかどうかは甚だ疑問であると思われており、経済的要因からはもう少し大きいところとも言われています。

研究テーマとしてはCMOS LSIの素子微細化の限界を見据えて、今後のLSIがハード、ソフトの両面から継続して発展していくためにはどういう技術を開発していくべきかを考えつつ、まずは微細シリコントランジスタ微細の特性研究、微細化限界とその打破(高誘電体ゲート絶縁膜などの新材料の導入、構造の改良等など)の研究などから手を染めていきたいと考えています。またその後のポストスケーリング時代に対応した、エマージング技術として、ゲルマニウムやⅢ-Ⅴ族半導体チャネル材料、シリコンナノワイヤートランジスタの研究を行っていこうと思っています。また、成果をできるだけ広く産業界に使っていただき、社会に貢献すること目指しており、産学連携と国際協力を研究の基本としています。

外部機関との連携研究



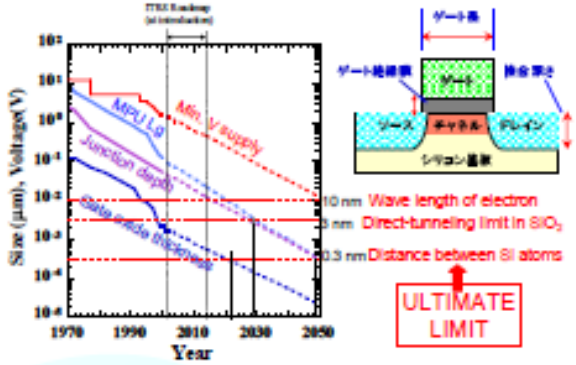
次世代高性能半導体デバイスに向けた研究テーマ

Siデバイスの重要性

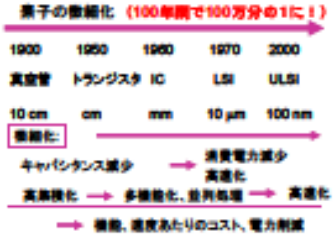
現代社会：生産、金融、運輸、医療、行政などの社会機構
インターネット、i-mode、Bluetooth、携帯電話、カーナビ、
ゲーム、自動車、航空機、製造装置などの全ての機器、
CD、DVDなどの娯楽

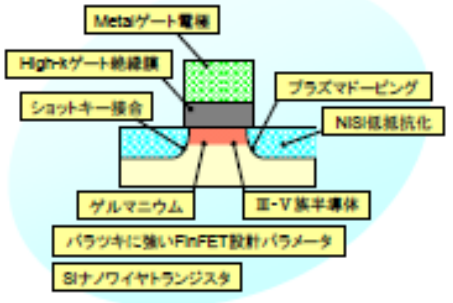
SI集積回路による管理・制御無くしてこれらは有り得ない

近年のSIデバイスの繁栄的な発展
- 数千万個ー数億個のトランジスタ集積
- MPUのクロック周波数　3GHz
- SiGeバイポーラのf_T300GHz以上

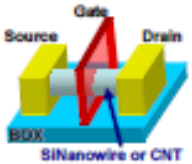


微細化の重要性



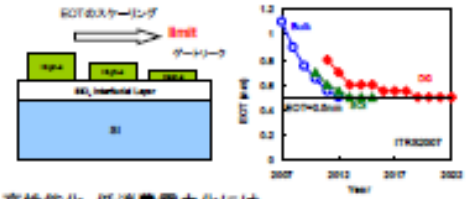


- ○低消費電力化
- ○高速性
- ○集積化
- ○バラツキ低減



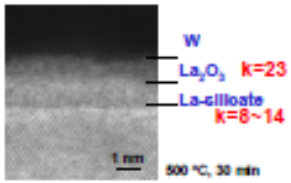
High-k/Metalゲートスタック

次世代ゲート絶縁膜材料として La_2O_3に注目

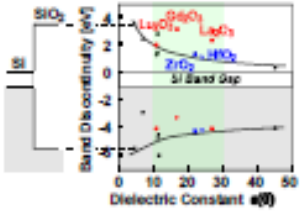


高性能化・低消費電力化には
EOT=0.5nmが必須

High-kとSiの直接接合が必要



La_2O_3は特性の良い直接接合が可能

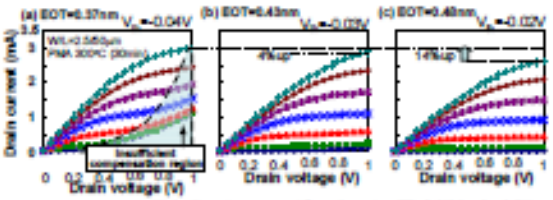


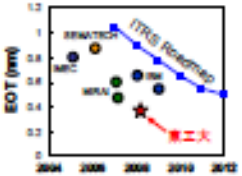
$$C_{ox}=\frac{\varepsilon_d\varepsilon_0}{t_{ox}}=\frac{\varepsilon_{SiO_2}\varepsilon_0}{EOT}\Rightarrow t_{ox}=\frac{\varepsilon_d}{\varepsilon_{SiO_2}}EOT$$

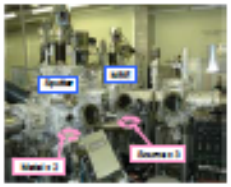
EOT : SiO_2等価換算膜厚

High-kゲート絶縁膜

EOT<0.4nmを達成



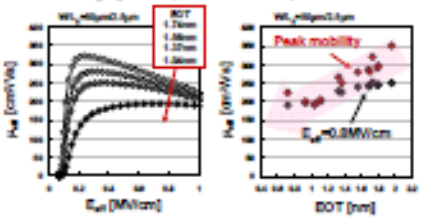




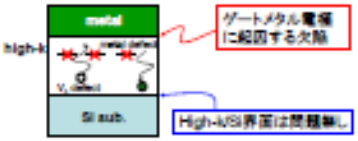
EOTの更なるスケーリングでドレイン電流増加を確認

低EOTにおける移動度劣化

W/La_2O_3/nFET, 500°C anneal, 30min in FG



直接接合で高い移動度を実現

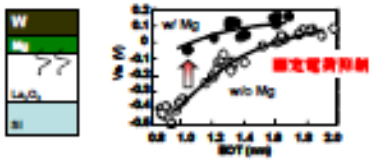


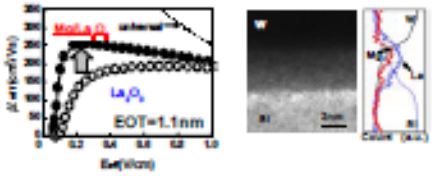
ゲートメタル電極に起因する
Coulomb散乱源の影響

低EOTの移動度向上技術

異種材料導入による低いEOTの移動度改善が可能

Mg(マグネシウム)の導入





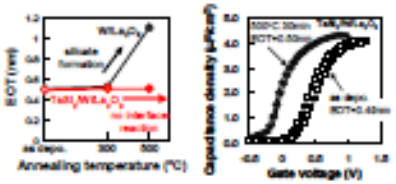
極限EOTに向けた材料選択

Metal Gate

$TaSi_2$を積層することで
酸素の侵入を抑制

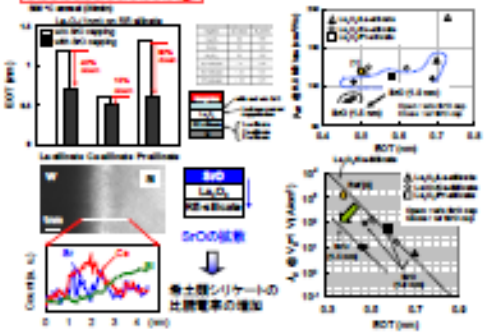
界面反応の抑制

500°CでEOT=0.5nmを達成



k-value boosting

Ce-silicateとSrO-cappingによって0.5nm EOTを達成



ゲルマニウムMOSFET

デバイスの更なる高速化のためにCMOSデバイスのチャネル材料としてGeが注目

ゲート長縮小の限界

$$I_{ds} = \frac{W}{L}\mu_{eff}C_{ox}\frac{1}{2}(V_g - V_{th})^2$$

	μ_h[cm²/Vs]	μ_e[cm²/Vs]
Si	1400	450
Ge	3900	1900
GaAs	8500	400
InP	4600	650

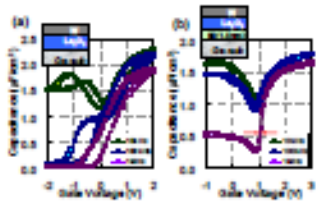
ソース・ドレイン間の漏れ電流増加

Geトランジスタのゲート絶縁膜

GeO_2は
①高温熱処理で分解
②水溶性（ウェットプロセス不可能）
③比誘電率が低い
→良好なトランジスタ特性が得られない

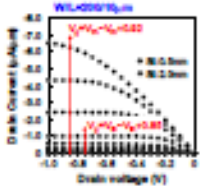
high-kをGeトランジスタの
ゲート絶縁膜として使おう!

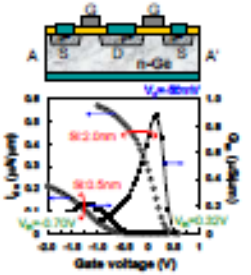
High-k/Ge界面の制御が重要



極薄Si挿入によりヒステリシスの低減が可能

W/La_2O_3/Ge p-MOSFET



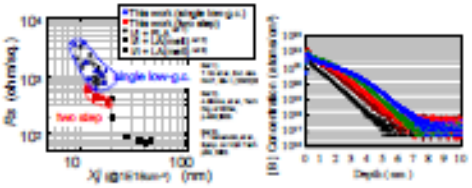


High-k/Geトランジスタの動作を確認

極浅接合用プラズマドーピング技術

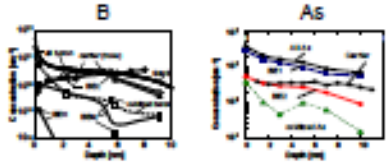
○低エネルギー注入(~100V)
○高いスループット(10^{15}cm^{-2}を30sec以内で注入可能)
○チャネリング無し→立体MOSFETに適用可能

極浅接合と高活性化の実現

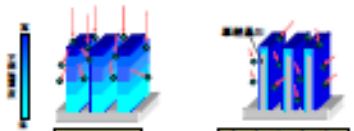


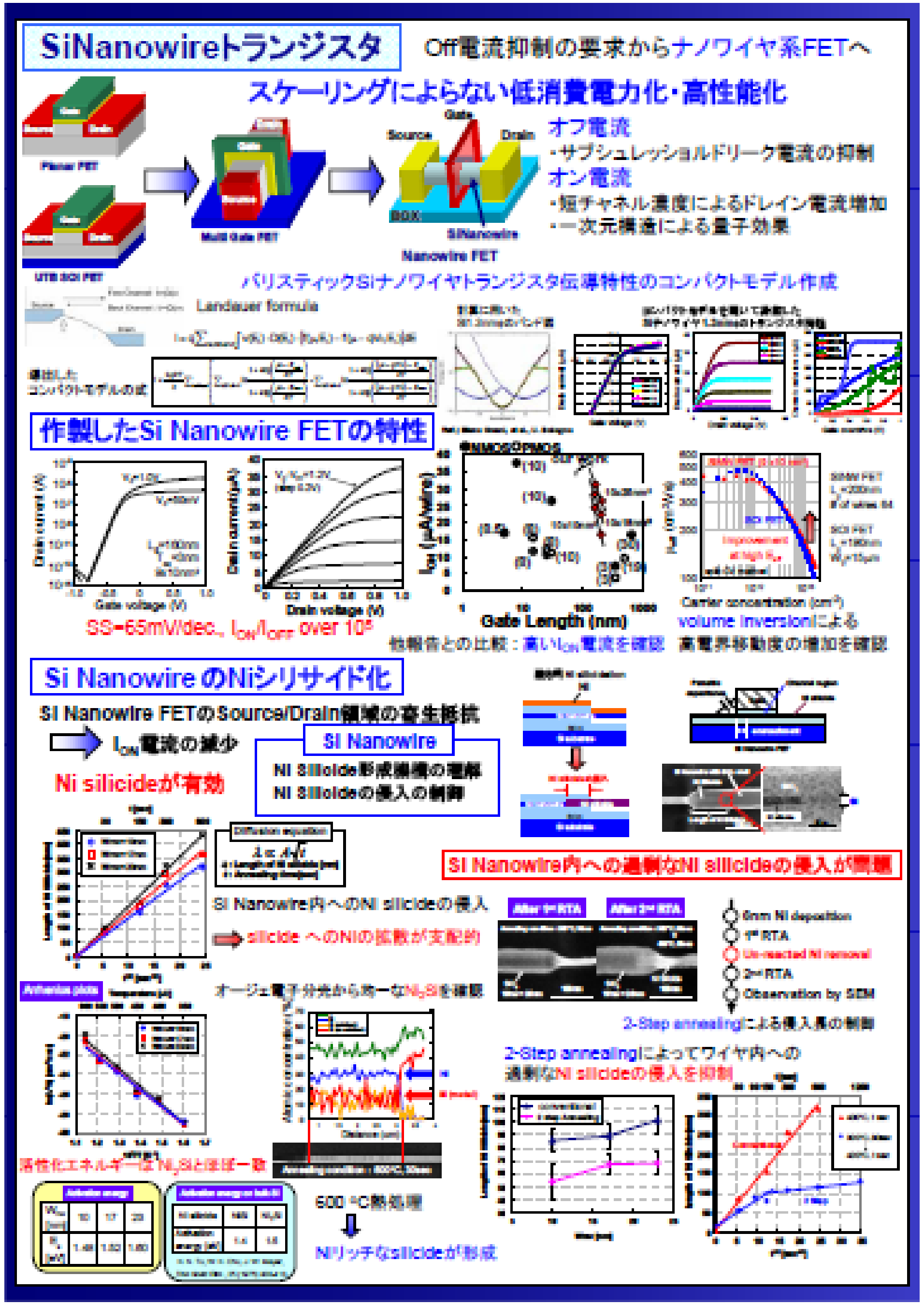
4nmの接合深さを実現
30%以上の高活性化率

Bの場合とAsの場合

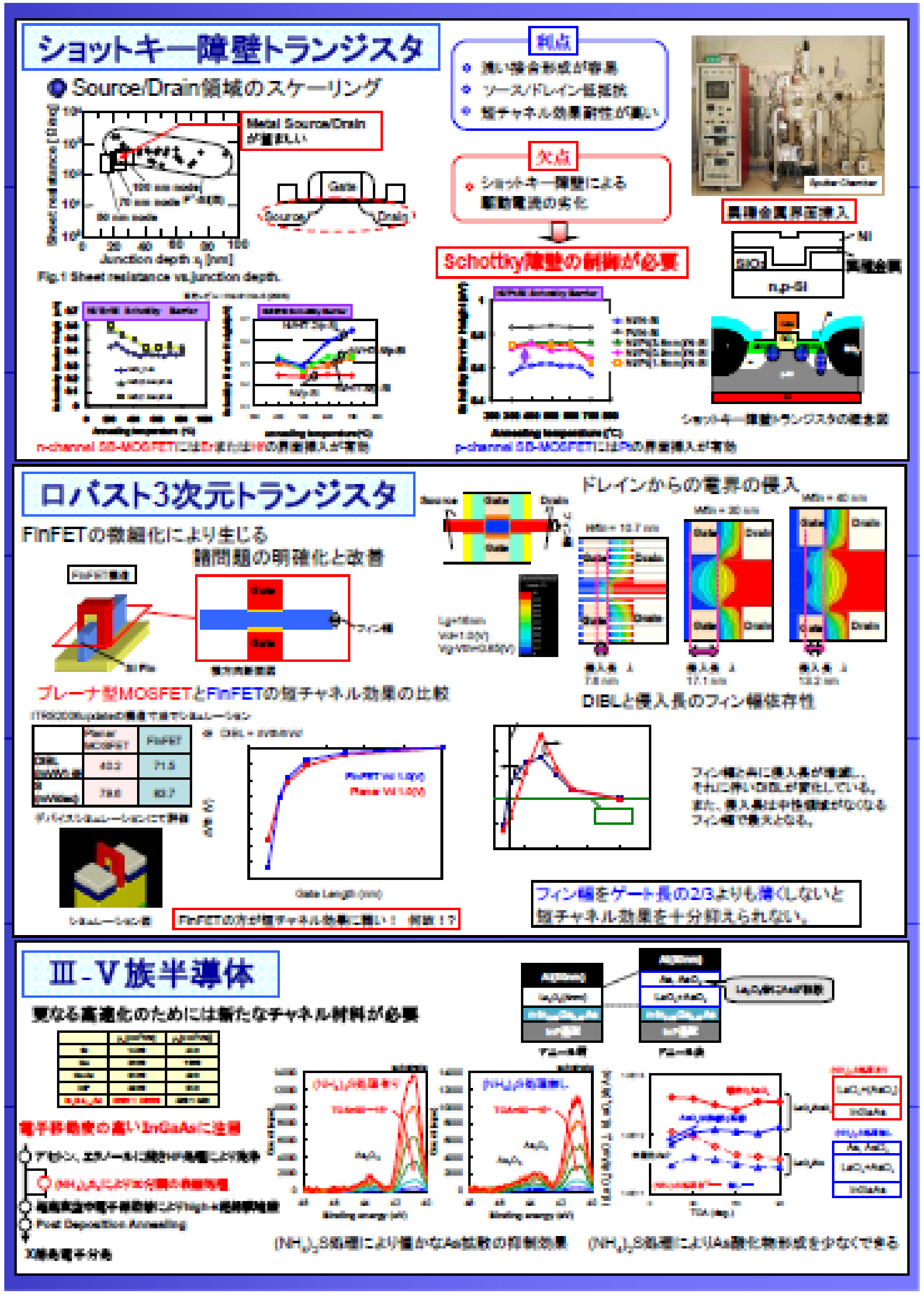


Fin構造へのプラズマドーピング





SiNanowireトランジスタ
Off電流抑制の要求からナノワイヤ系FETへ
スケーリングによらない低消費電力化・高性能化
Planar FET
UTB SOI FET
Multi Gate FET
Nanowire FET
オフ電流
・サブシュレッショルドリーク電流の抑制
オン電流
・短チャネル濃度によるドレイン電流増加
・一次元構造による量子効果
バリスティックSiナノワイヤトランジスタ伝導特性のコンパクトモデル作成
Landauer formula
作製したSi Nanowire FETの特性
Gate voltage (V)
Drain voltage (V)
SS=65mV/dec., I_{ON}/I_{OFF} over 10^5
NMOS PMOS
Gate Length (nm)
Carrier concentration (cm^{-3})
volume inversionによる
高電界移動度の増加を確認
Si Nanowire のNiシリサイド化
Si Nanowire FETのSource/Drain領域の寄生抵抗
I_{ON}電流の減少
Ni silicideが有効
Si Nanowire
Ni Silicide形成機構の理解
Ni Silicideの侵入の制御
Diffusion equation
Si Nanowire内への過剰なNi silicideの侵入が問題
Si Nanowire内へのNi silicideの侵入
silicide へのNiの拡散が支配的
After 1st RTA
After 2nd RTA
Arrhenius plots
オージェ電子分光から均一なNi_2Siを確認
1st RTA
Un-reacted Ni removal
2nd RTA
Observation by SEM
2-Step annealingによる侵入長の制御
2-Step annealingによってワイヤ内への
過剰なNi silicideの侵入を抑制
活性化エネルギーはNi_2Siとほぼ一致
500 °C熱処理
Niリッチなsilicideが形成



ショットキー障壁トランジスタ
Source/Drain領域のスケーリング
利点
浅い接合形成が容易
ソース/ドレイン低抵抗
短チャネル効果耐性が高い
欠点
ショットキー障壁による
駆動電流の劣化
Metal Source/Drain
Schottky障壁の制御が必要
異種金属界面挿入
Junction depth x_j [nm]
Fig.1 Sheet resistance vs.junction depth.
n-channel SB-MOSFETにはErまたはHfの界面挿入が有効
p-channel SB-MOSFETにはPtの界面挿入が有効
ショットキー障壁トランジスタの概念図
ロバスト3次元トランジスタ
FinFETの微細化により生じる
諸問題の明確化と改善
ドレインからの電界の侵入
DIBLと侵入長のフィン幅依存性
プレーナ型MOSFETとFinFETの短チャネル効果の比較
FinFETの方が短チャネル効果に強い！ 何故！？
フィン幅をゲート長の2/3よりも薄くしないと
短チャネル効果を十分抑えられない。
Ⅲ-Ⅴ族半導体
更なる高速化のためには新たなチャネル材料が必要
電子移動度の高いInGaAsに注目
Post Deposition Annealing
Binding energy (eV)
$(NH_4)_2S$処理により僅かなAs拡散の抑制効果
$(NH_4)_2S$処理によりAs酸化物形成を少なくできる

Importance of Electronics

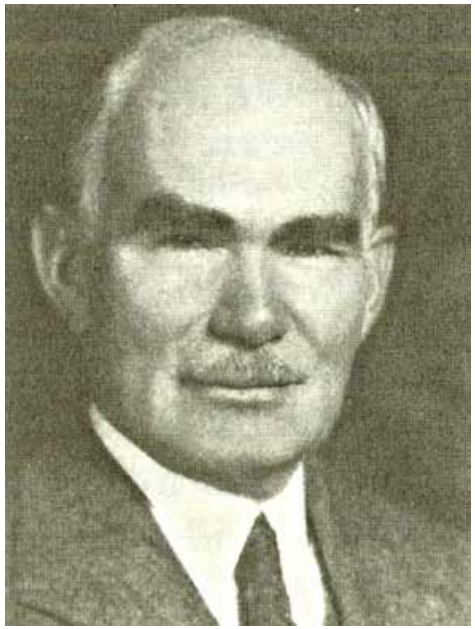
- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

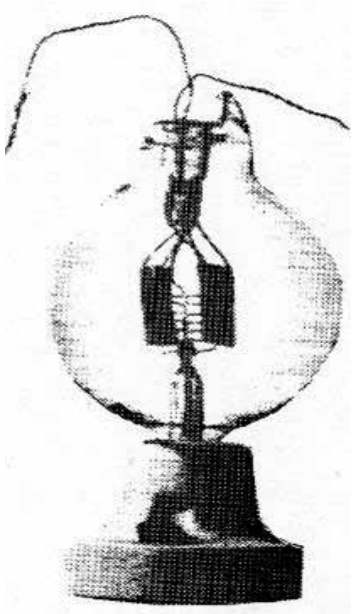
  Space aircraft, etc
- However, everything has to be controlled by electronics
- Electronics

  Most important invention in the 20th century
- What is Electronics: To use electrons,

  Electronic Circuits

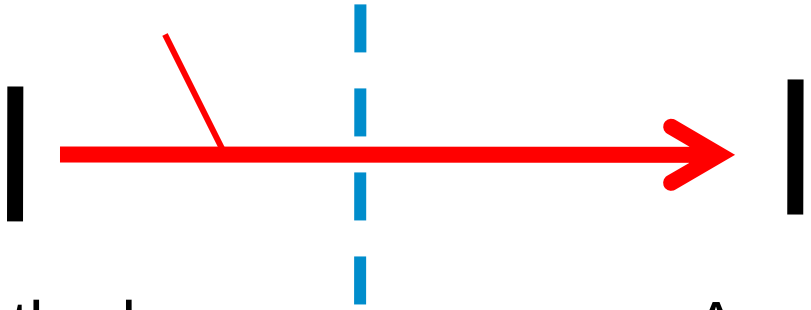


Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

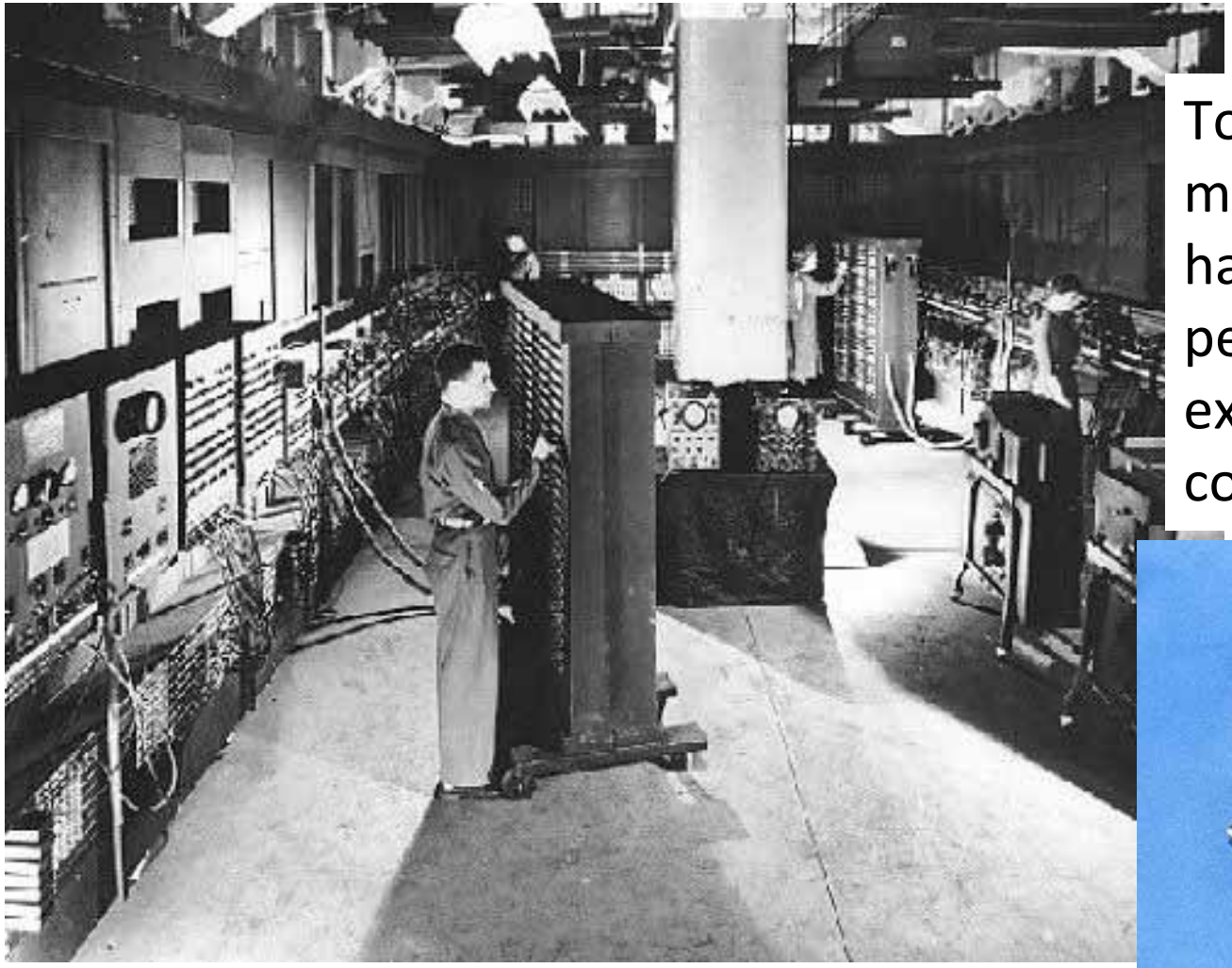
Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

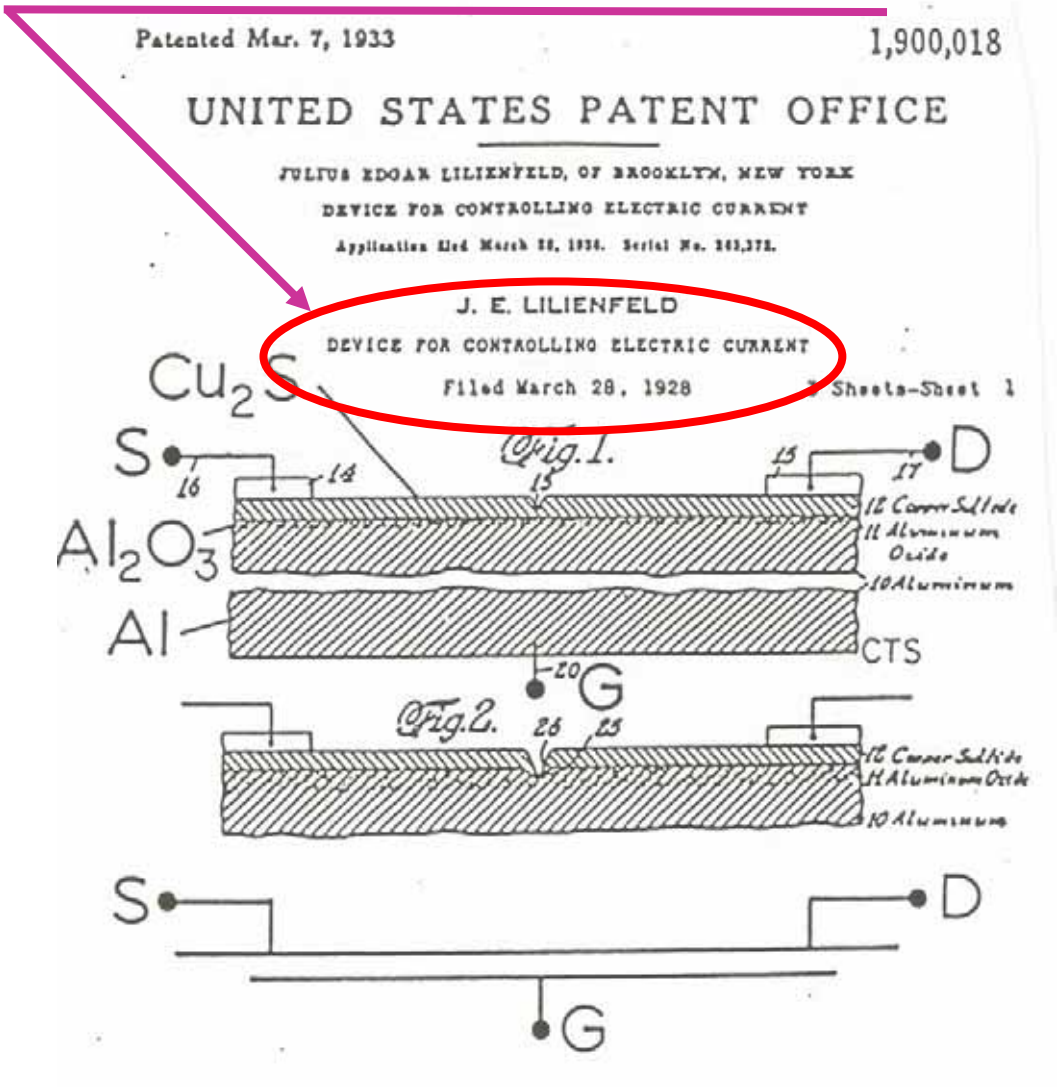


Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March 28, 1928. Serial No. 263,372.

J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 2 Sheets-Sheet 1

Cu_2S

S

D

Al_2O_3

Al

CTS

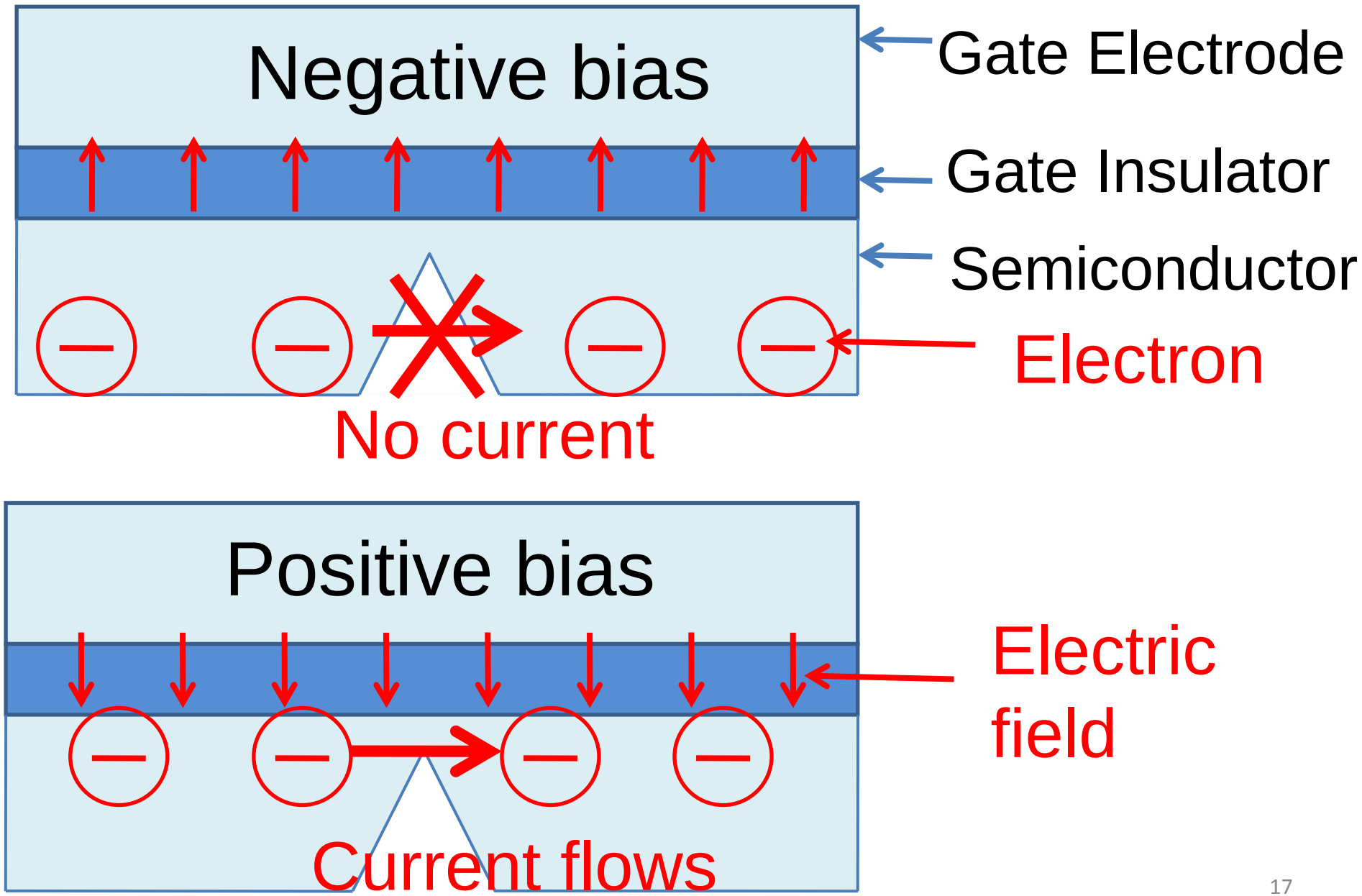
G

Fig. 1.

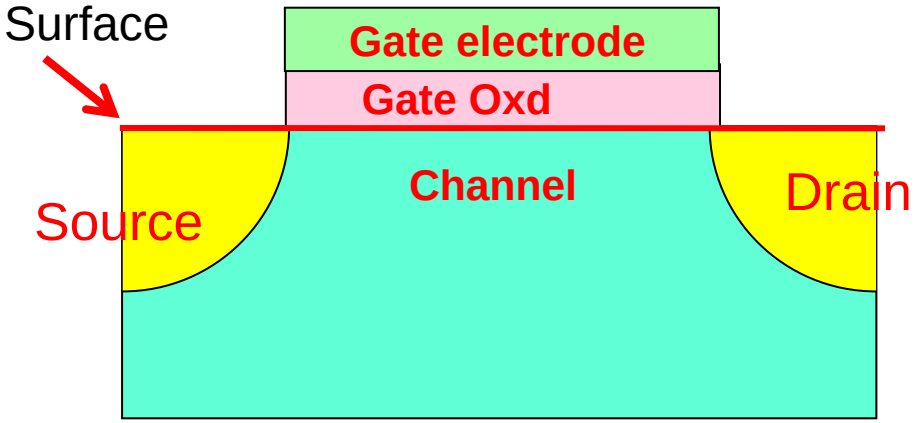
Fig. 2.

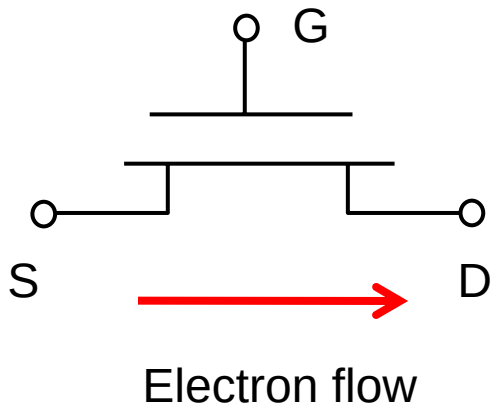
J.E.LILIENFELD

Capacitor structure with notch



Today's transistor: MOSFET for CMOS LSI

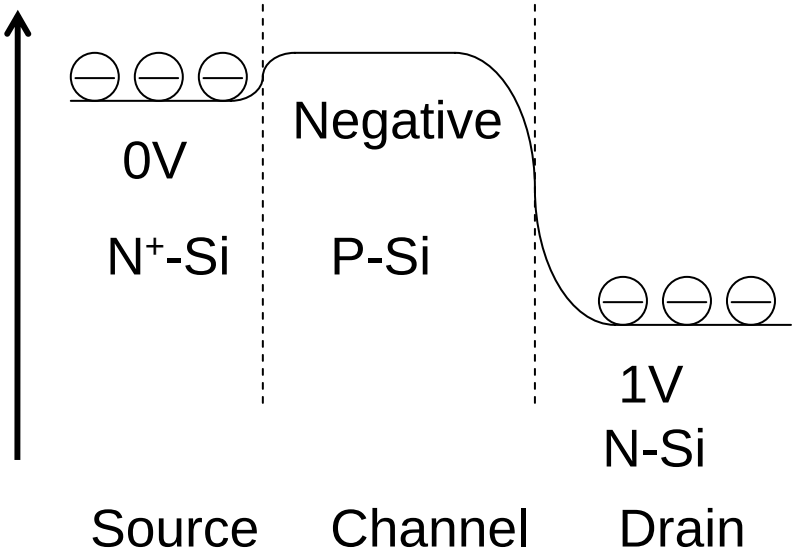


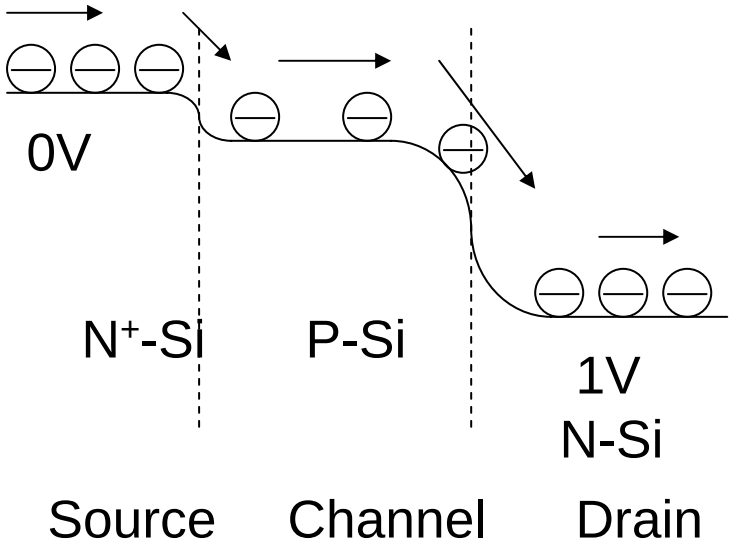


0 bias for gate

Positive bias for gate

Surface Potential (Negative direction)



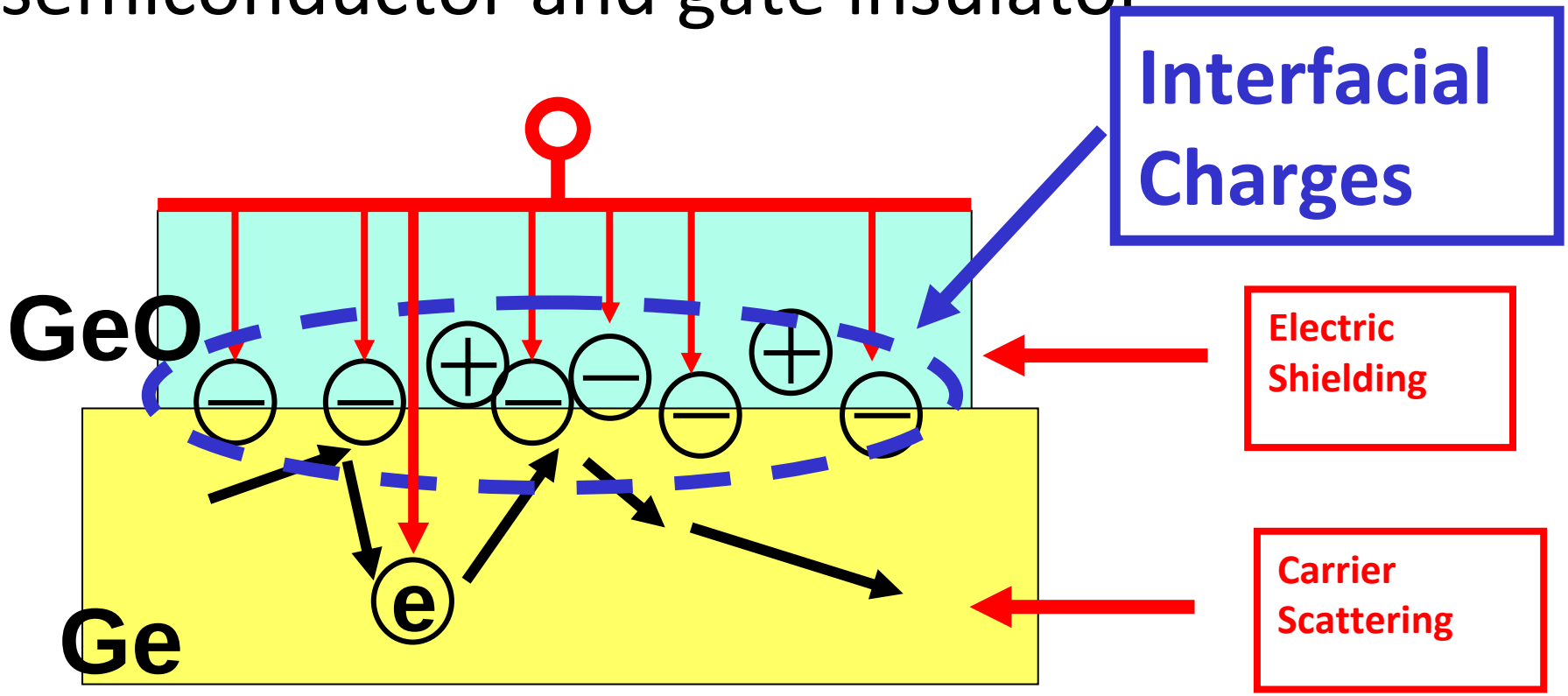


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator

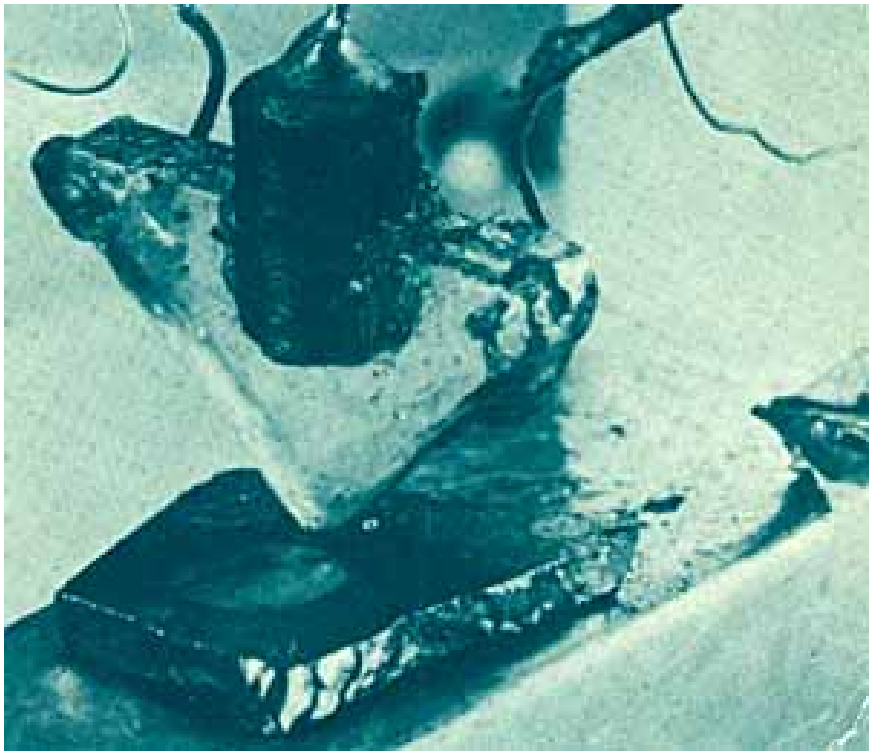


Drain Current was several orders of magnitude smaller than expected

Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.
This is the 1st Transistor:
Not Field Effect Transistor,
But Bipolar Transistor (another mechanism)

1947: 1st transistor



Bipolar using Ge

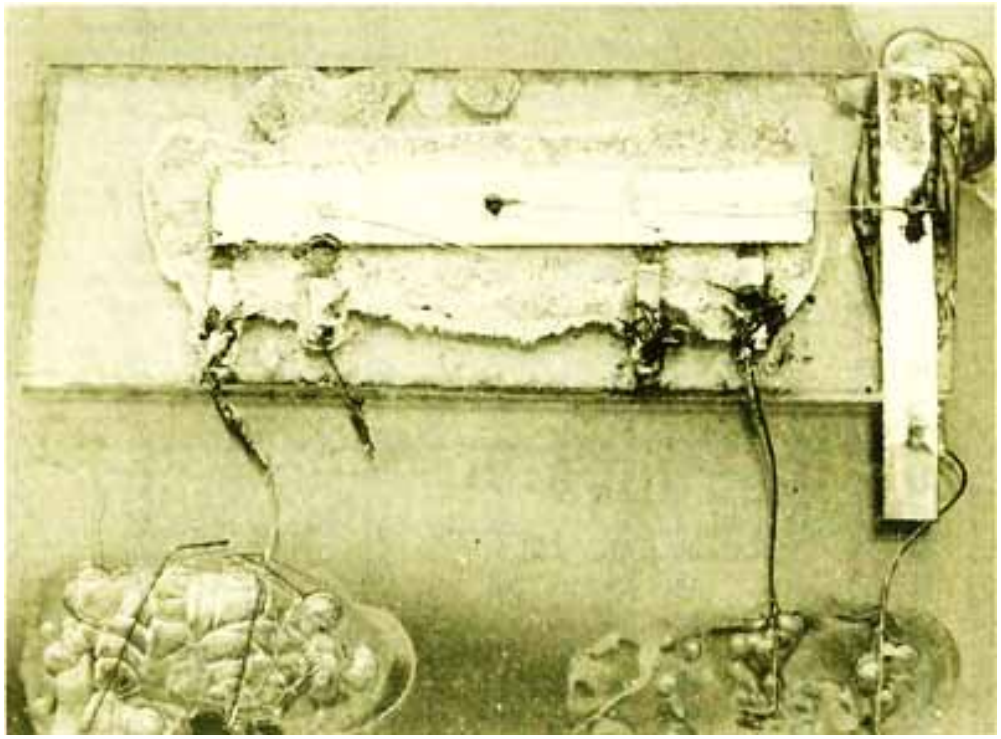
J. Bardeen W. Bratten,

W. Shockley

1958: 1st Integrated Circuit

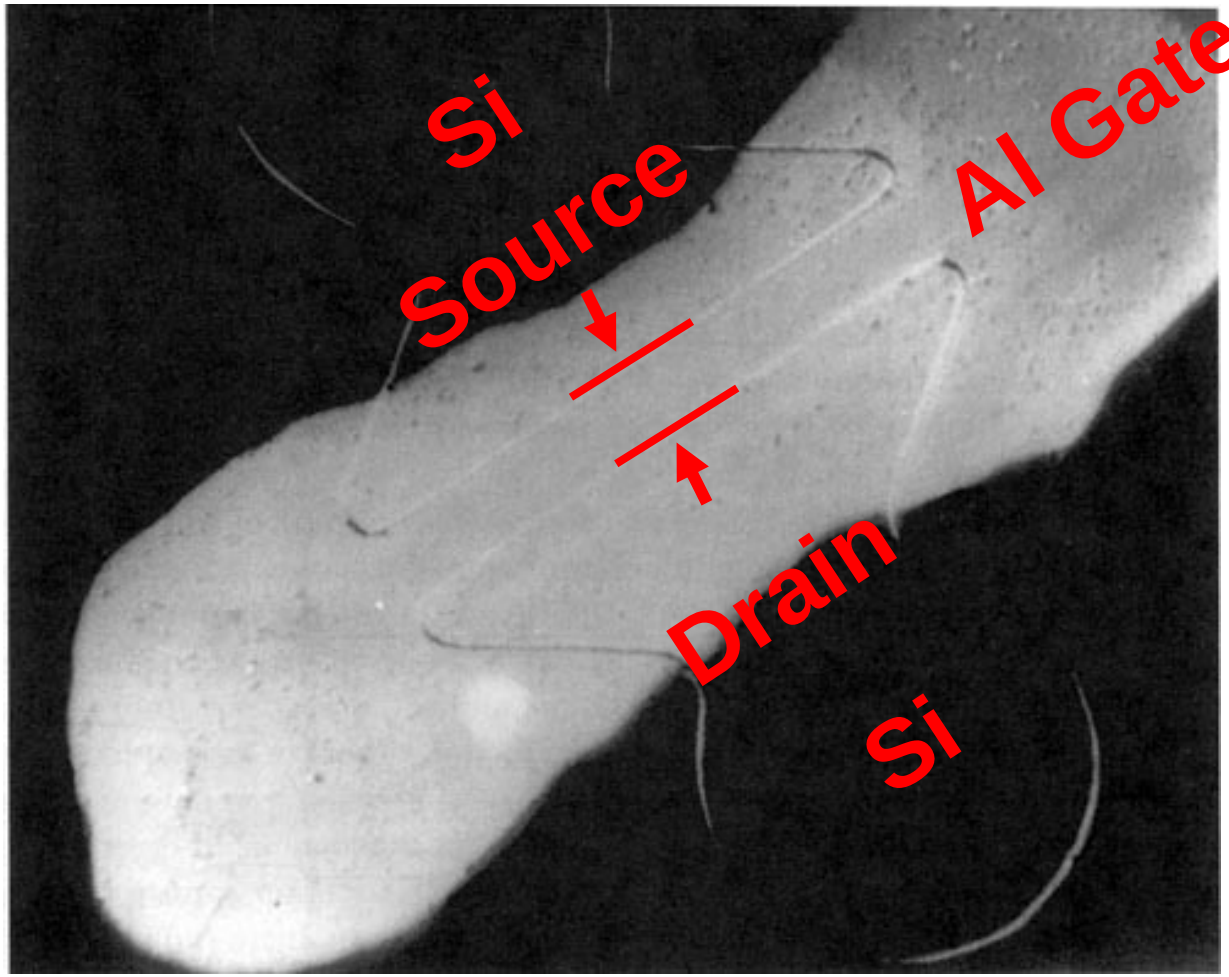
Jack S. Kilby

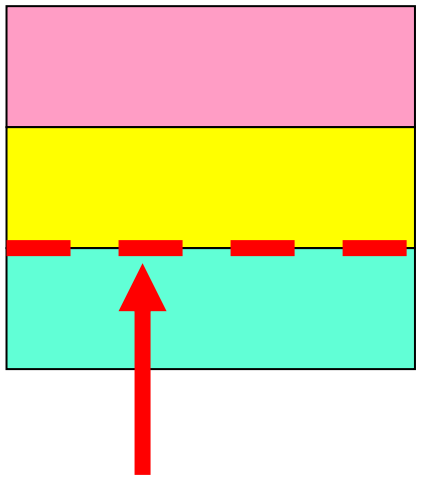
Connect 2 bipolar transistors in the
Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

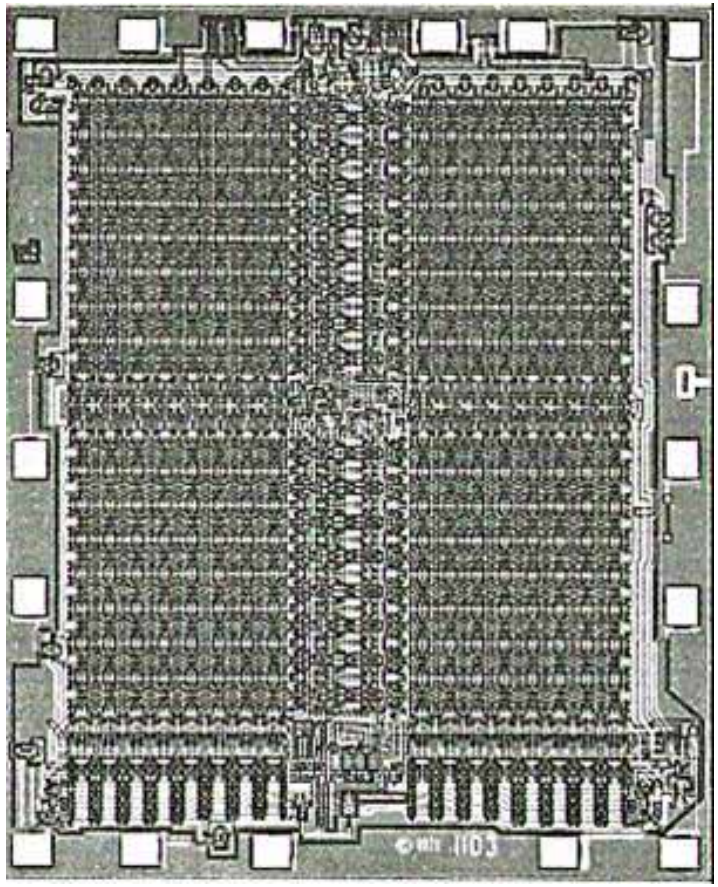
Top View



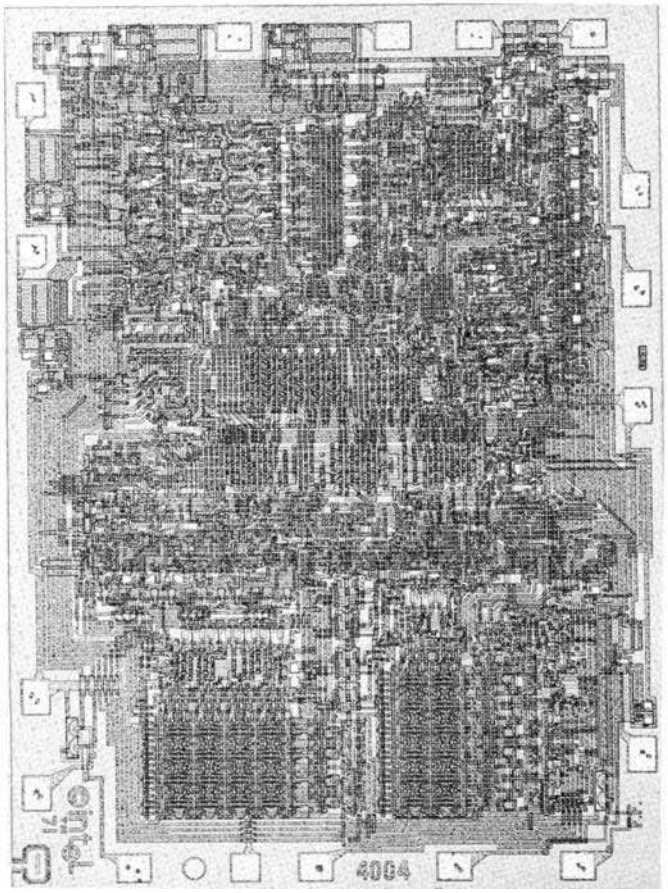


1970,71: 1st generation of LSIs

DRAM Intel 1103

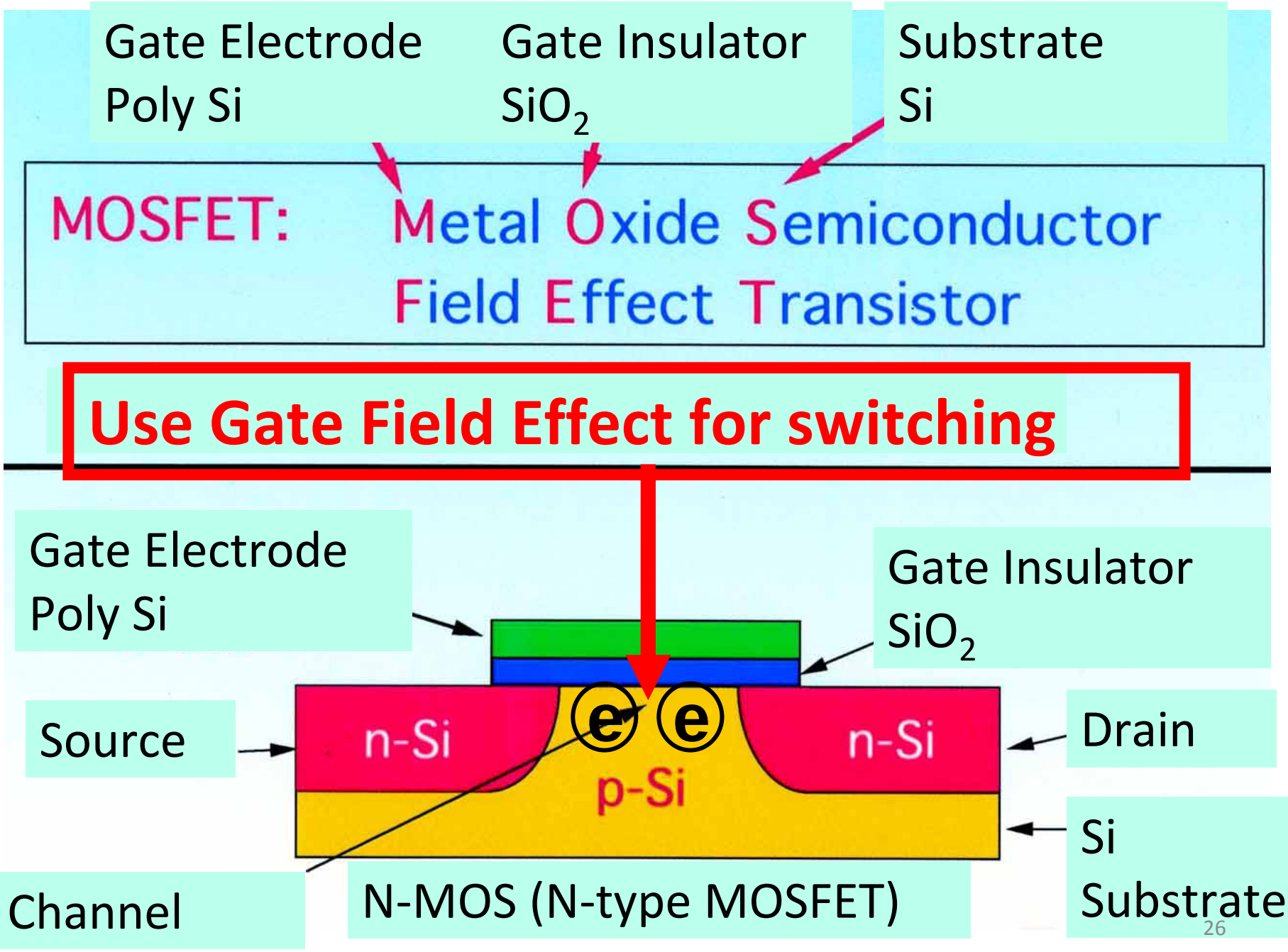


MPU Intel 4004



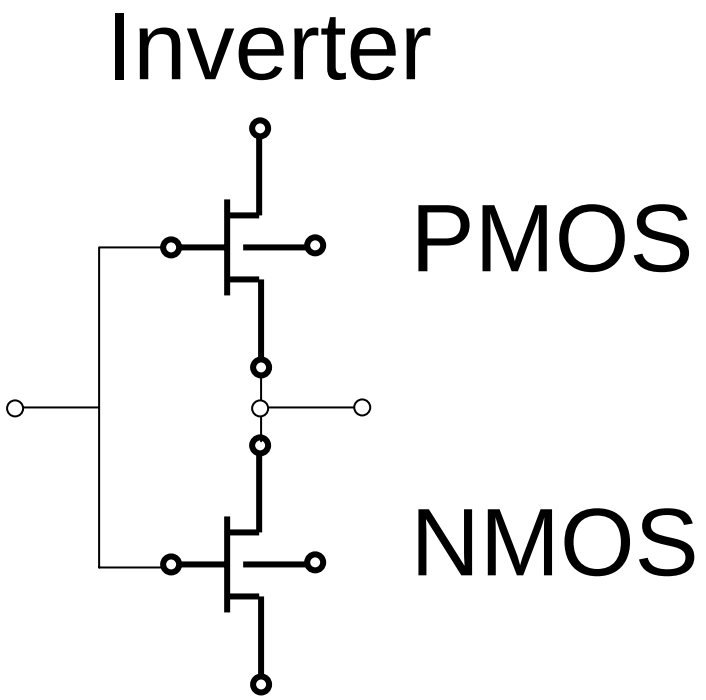
MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000


Gate Electrode
Poly Si
Gate Insulator
SiO2
Substrate
Si
MOSFET: Metal Oxide Semiconductor
Field Effect Transistor
Use Gate Field Effect for switching
Gate Electrode
Poly Si
Gate Insulator
SiO2
Source
n-Si
e
e
n-Si
Drain
p-Si
Si
Substrate
Channel
N-MOS (N-type MOSFET)

CMOS

Complimentary MOS



When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

Needless to say, but….

CMOS Technology:

Indispensible for our human society

Al the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

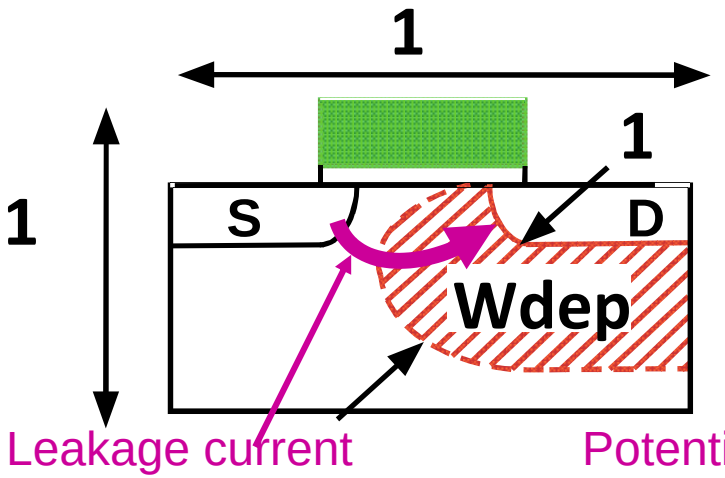
→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

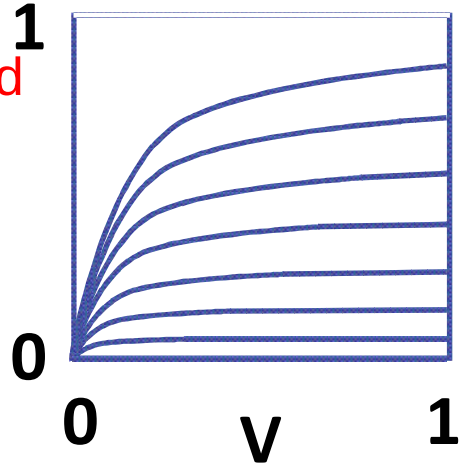
Thus, downsizing of Si devices is the most important and critical issue.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

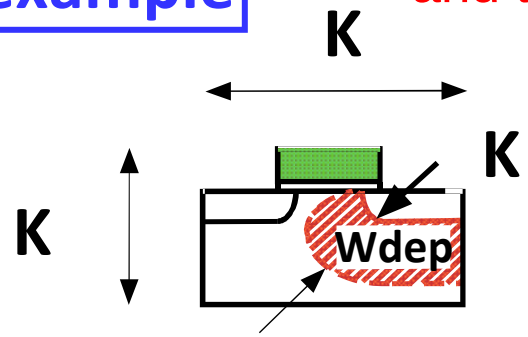
Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

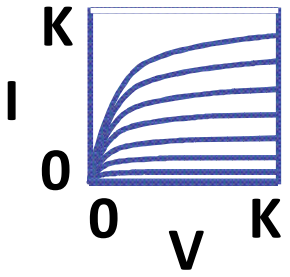
X , Y , Z : K, V : K, Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$Wdep \propto \sqrt{V/Na}$$
$$: K$$



I : K

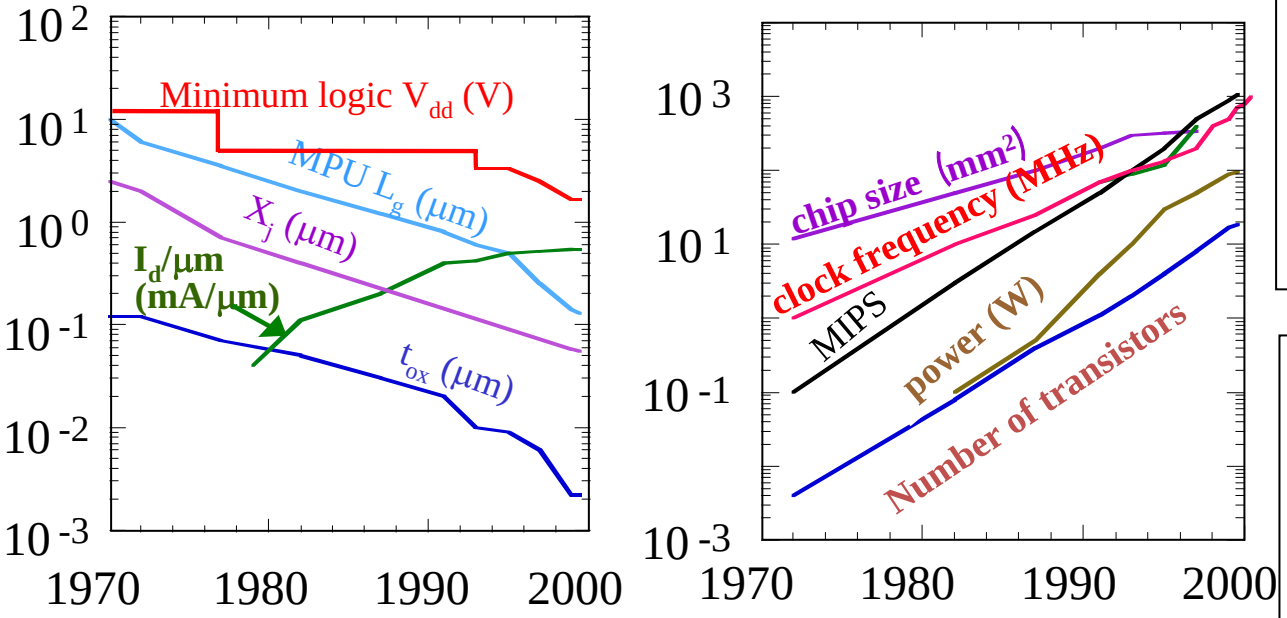
31

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area → $W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ → KK/K = K
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d$ → KK/K= K
Clock frequency	f	1/K	$f = 1/\tau$ = 1/K
Chip area	A_{chip}	α	α: Scaling factor → **In the past, $\alpha>1$ for most cases**
Integration (# of Tr)	N	α/K^2	N → α/K^2 **= $1/K^2$, when $\alpha=1$**
Power per chip	P	α	$fNCV^2/2$ → $K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **= 1, when $\alpha=1$**

k= 0.7 and α =1	k= 0.7^2 =0.5 and α =1
Single MOFET	
Vdd → 0.7 Lg → 0.7 Id → 0.7 Cg → 0.7	Vdd → 0.5 Lg → 0.5 Id → 0.5 Cg → 0.5
P (Power)/Clock → $0.7^3 = 0.34$ τ (Switching time) → 0.7	P (Power)/Clock → $0.5^3 = 0.125$ τ (Switching time) → 0.5
Chip	
N (# of Tr) → $1/0.7^2 = 2$ f (Clock) → 1/0.7 = 1.4 P (Power) → 1	N (# of Tr) → $1/0.5^2 = 4$ f (Clock) → 1/0.5 = 2 P (Power) → 1

Actual past downscaling trend until year 2000



Source. Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Past 30 years scaling

Merit: N, f increase

Demerit: P increase

V_{dd} scaling insufficient

⇩

Additional significant increase in I_d, f, P

Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
L_g	K	10^{-2}	I_d	K (10^{-2})	10^{-1}	f	1/K(10^{2})	10^{3}
t_{ox}	K(10^{-2})	10^{-2}						
V_{dd}	K(10^{-2})	10^{-1}	I_d/μm	1	10^{1}	P	α(10^{1})	10^{5}
						= fαNCV²		
A_{chip}	α	10^{1}	N	α/K²(10^{5})	10^{4}			

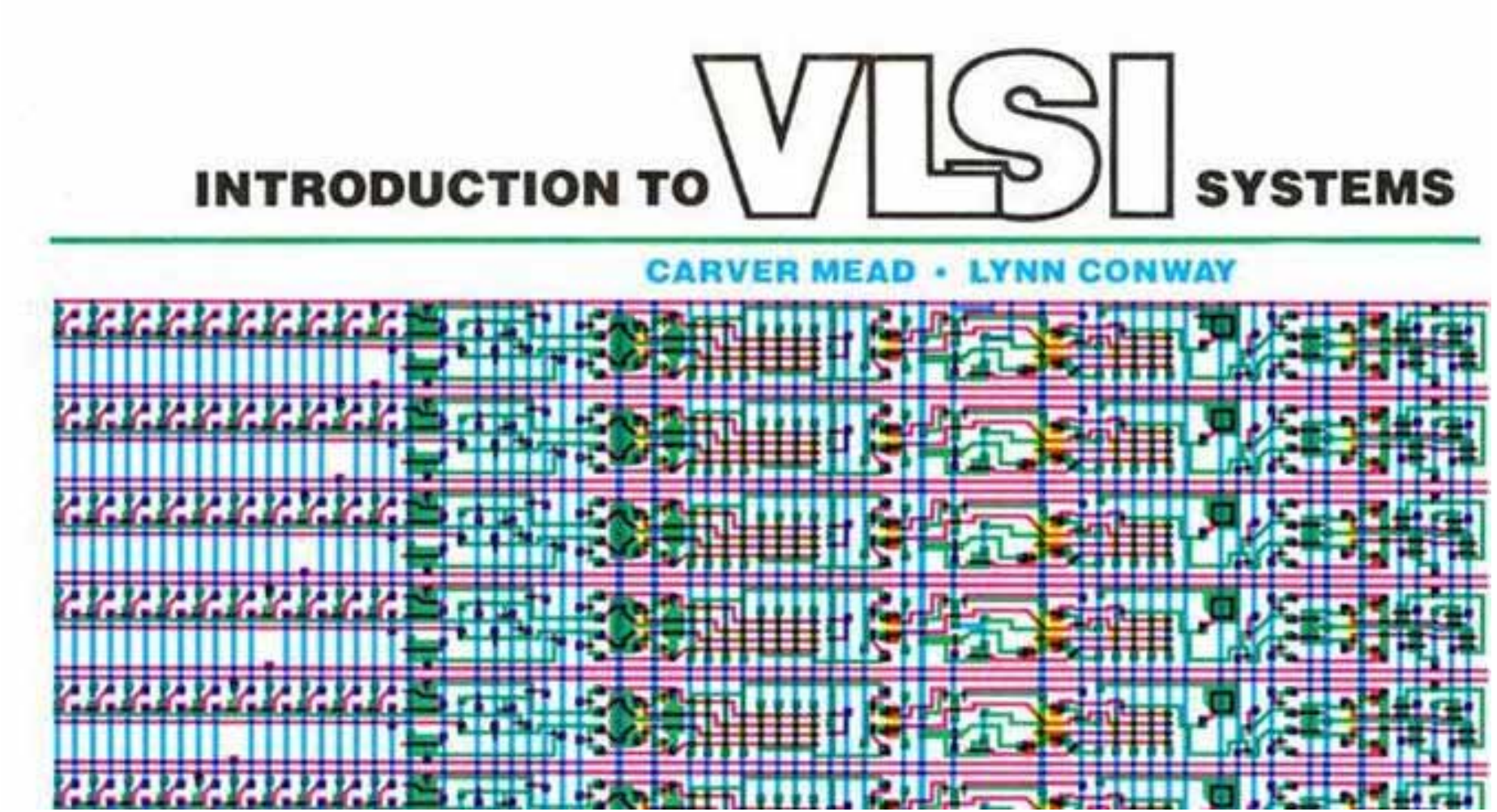
Vd scaling insufficient, α increased → N, Id, f, P increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

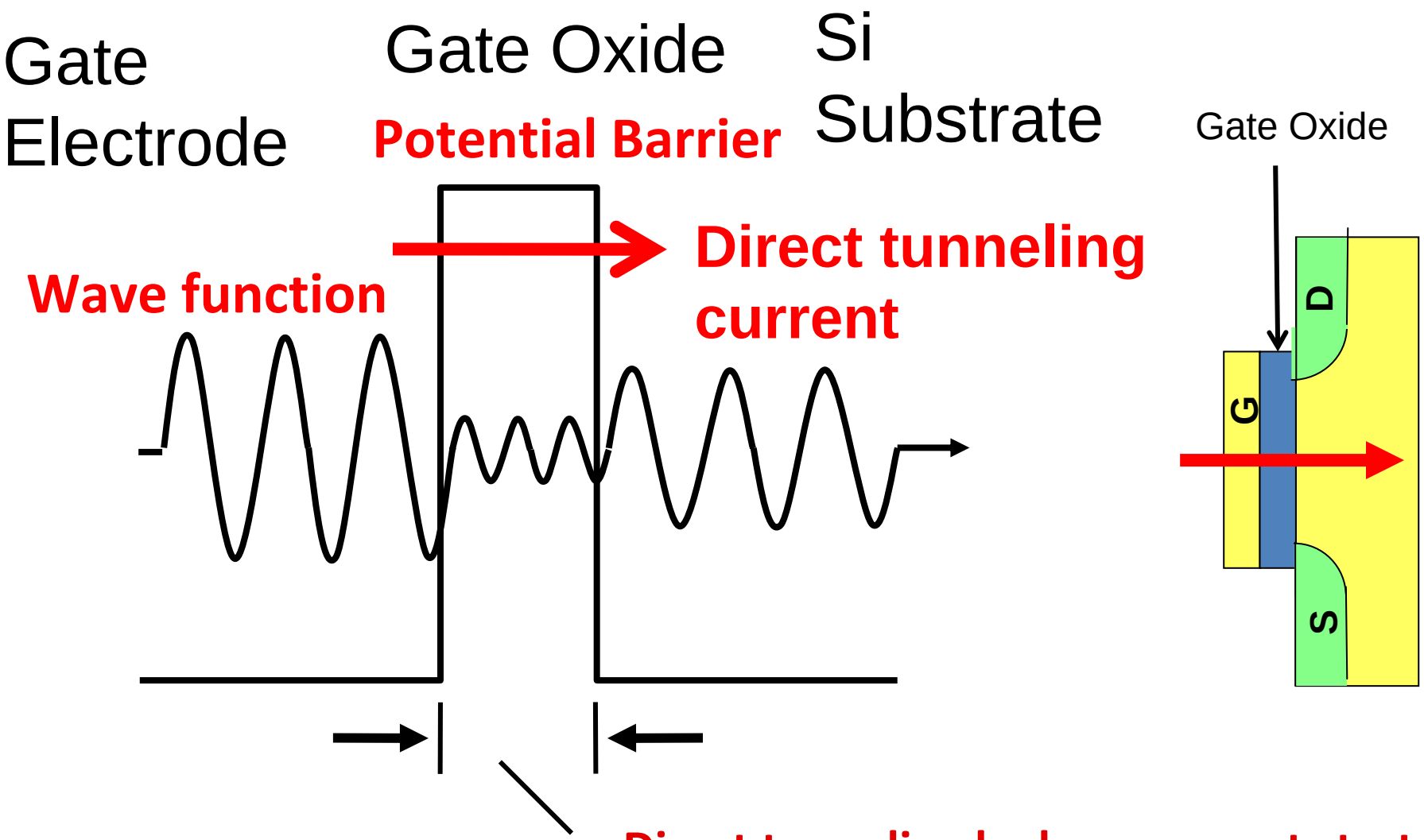


C. Mead L. Conway

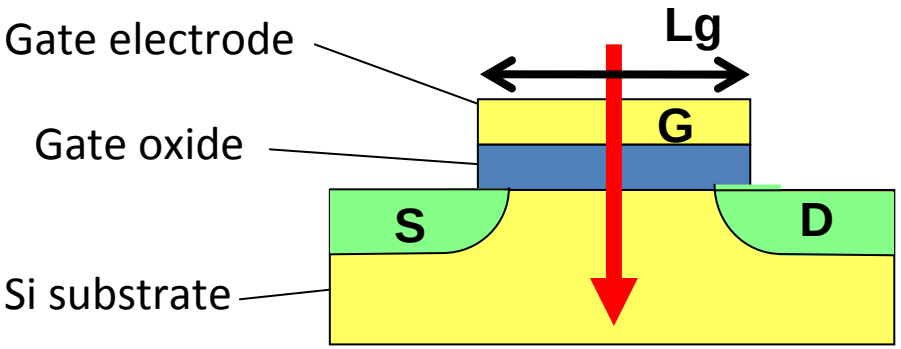
VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect

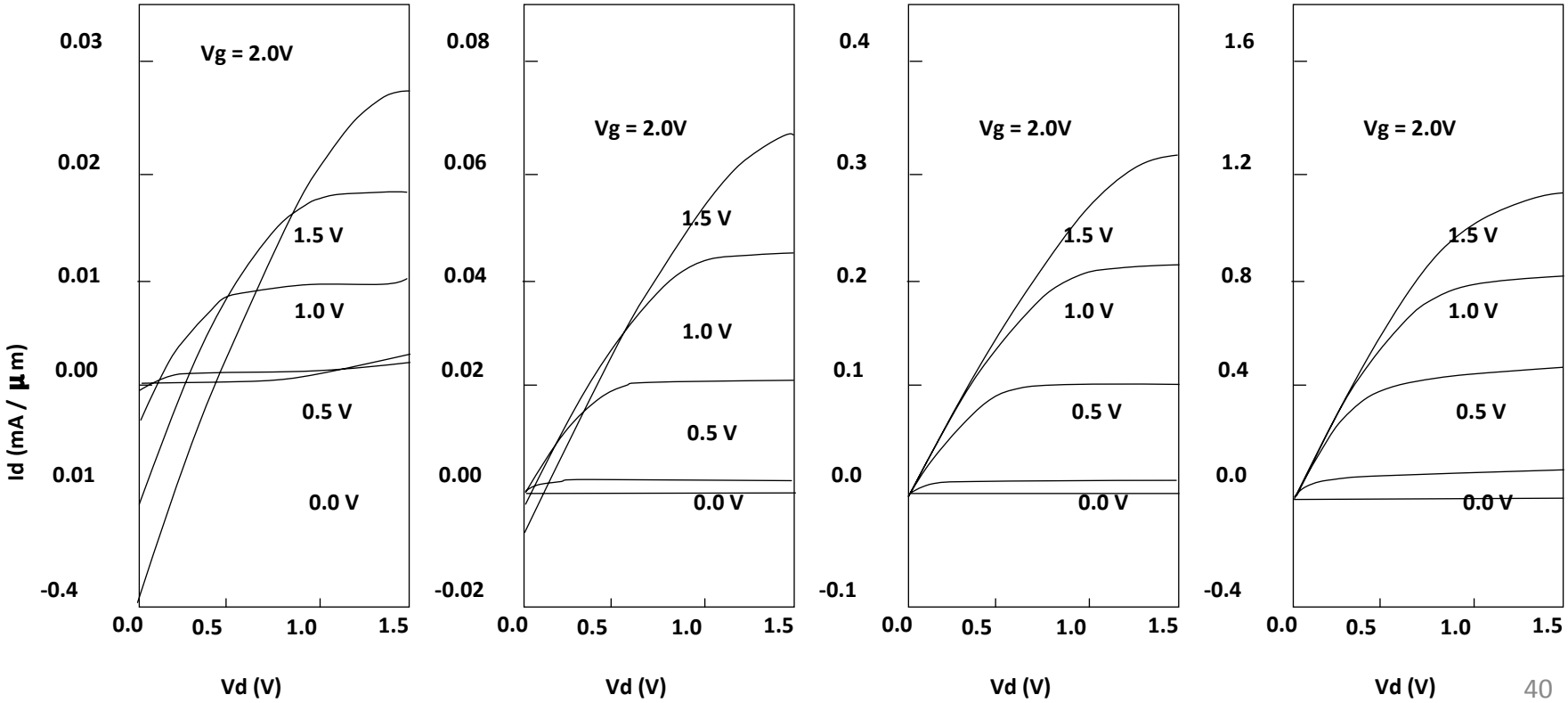


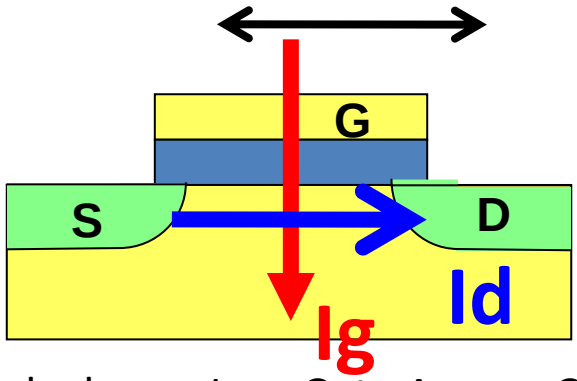
Direct tunneling leakage current start to flow when the thickness is 3 nm.



Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide



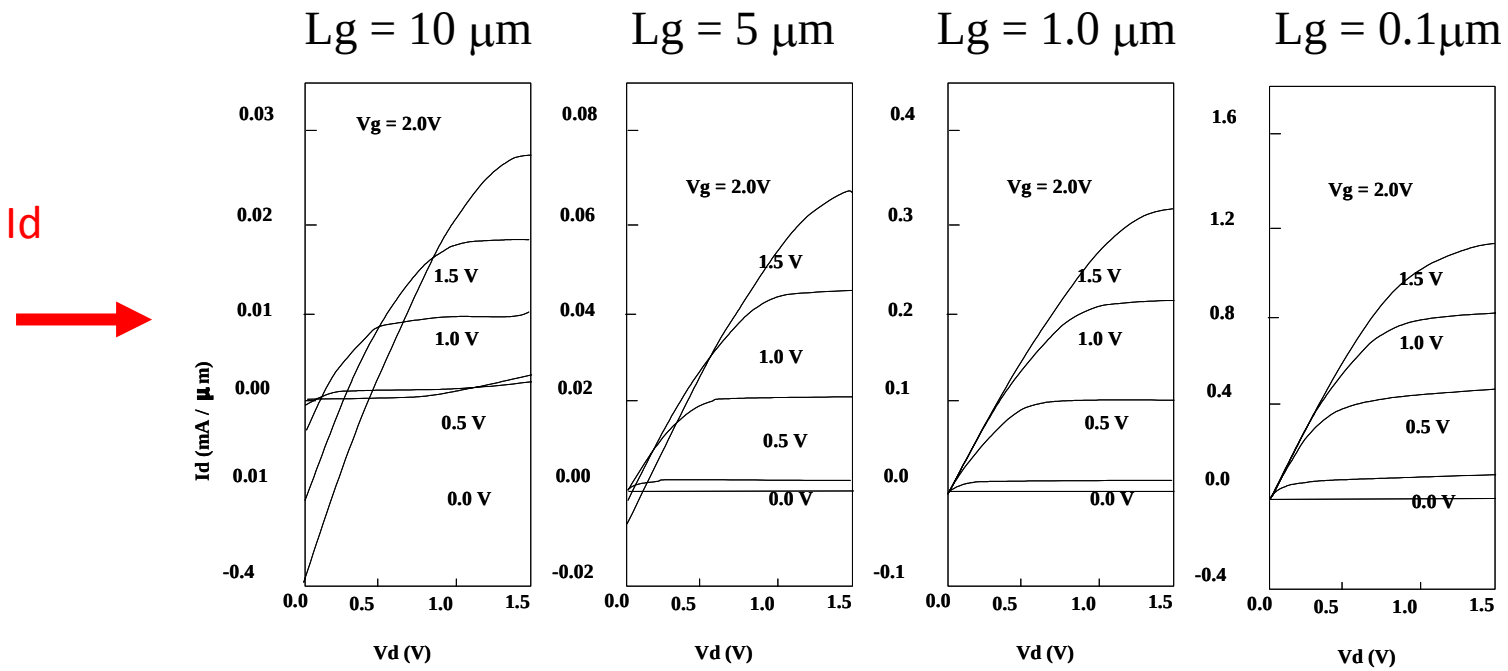


Gate leakage: Ig ∝ Gate Area ∝ Gate length (Lg)

Drain current: Id ∝ 1/Gate length (Lg)

Lg → small,

Then, Ig → small, Id → large, Thus, Ig/Id → very small



Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

Transistor Scaling Continues

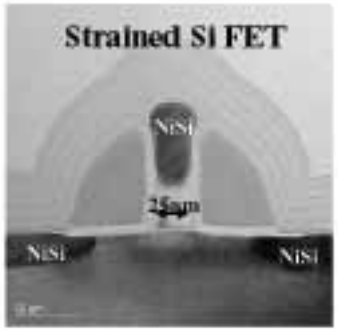
90nm node

Lg=50nm

65nm node

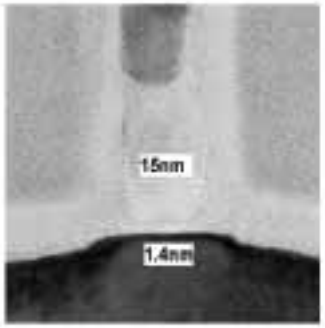
Lg=35nm

45nm node



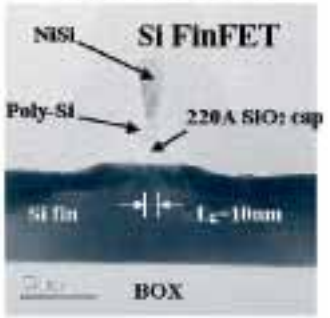
Lg=25nm

32nm node

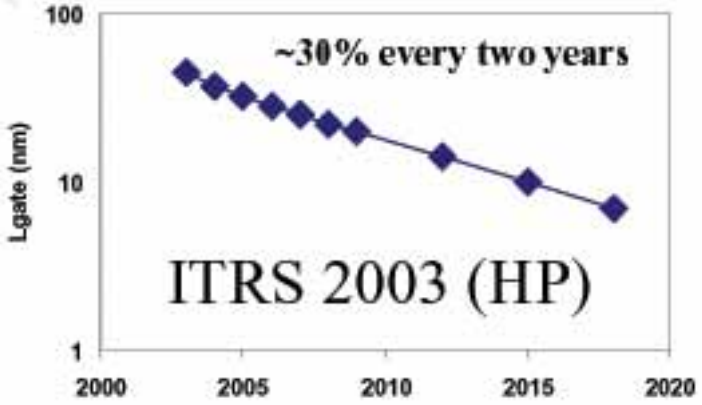


Lg=15nm

22nm node



Lg=10nm

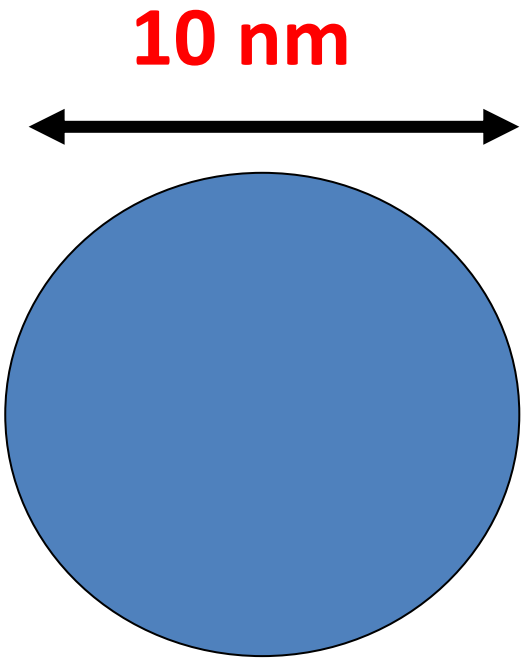


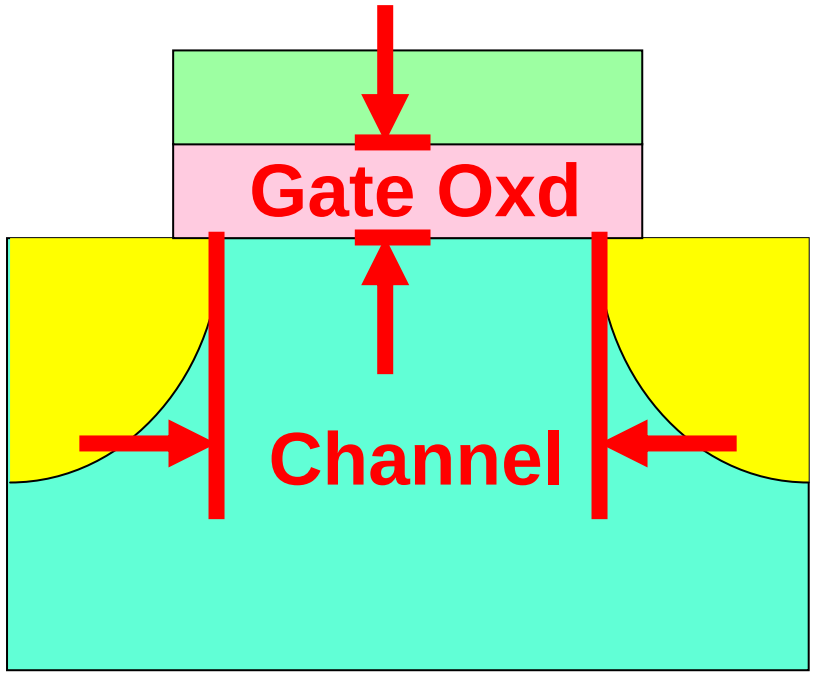
Qi Xinag, ECS 2004, AMD

Downsizing limit?

Channel length?

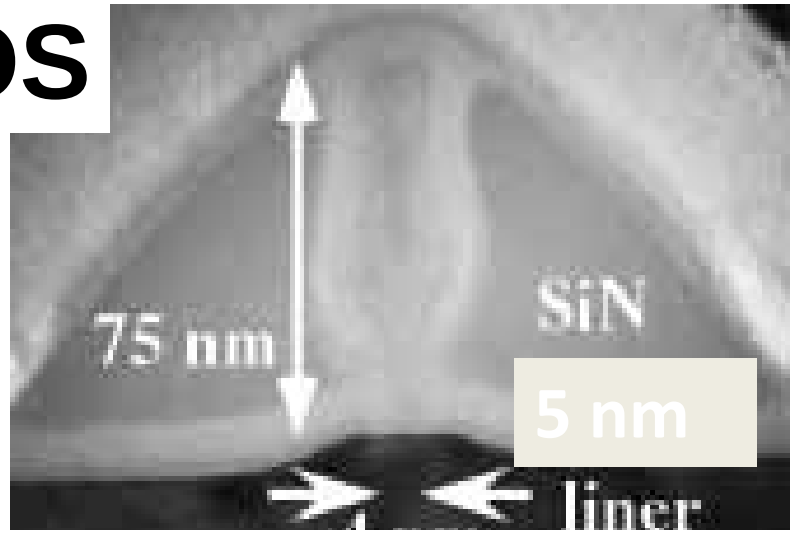
Electron wave length



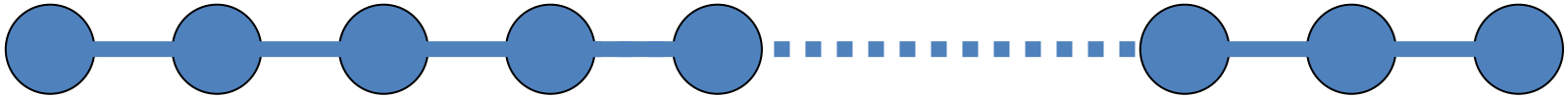


5 nm gate length CMOS

Is a Real Nano Device!!

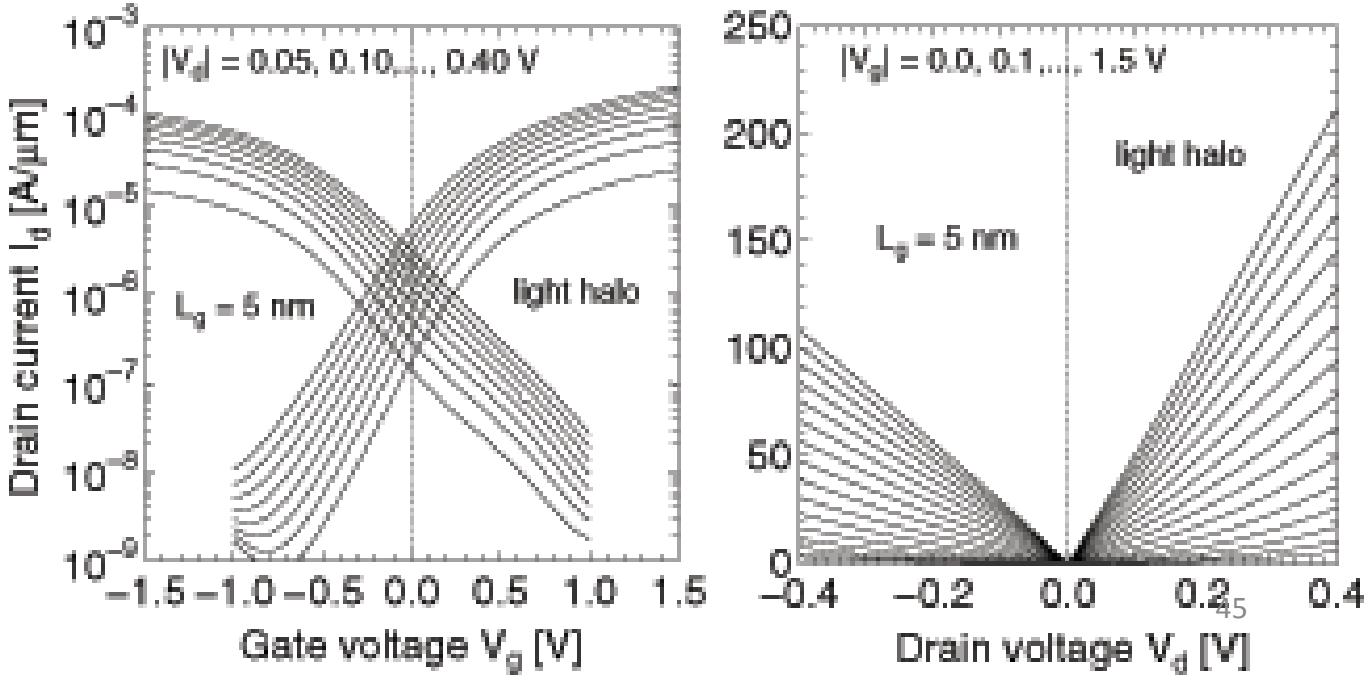


Length of 18 Si atoms



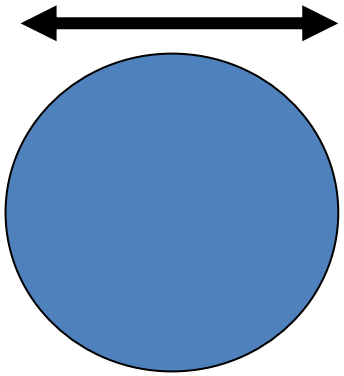
H. Wakabayashi
et.al, NEC

IEDM, 2003



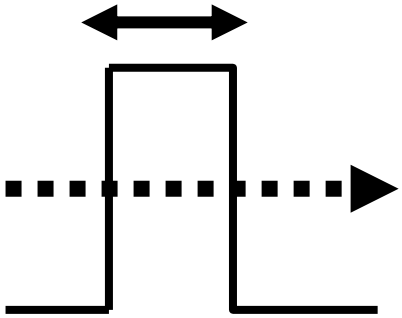
Electron wave length

10 nm



Tunneling distance

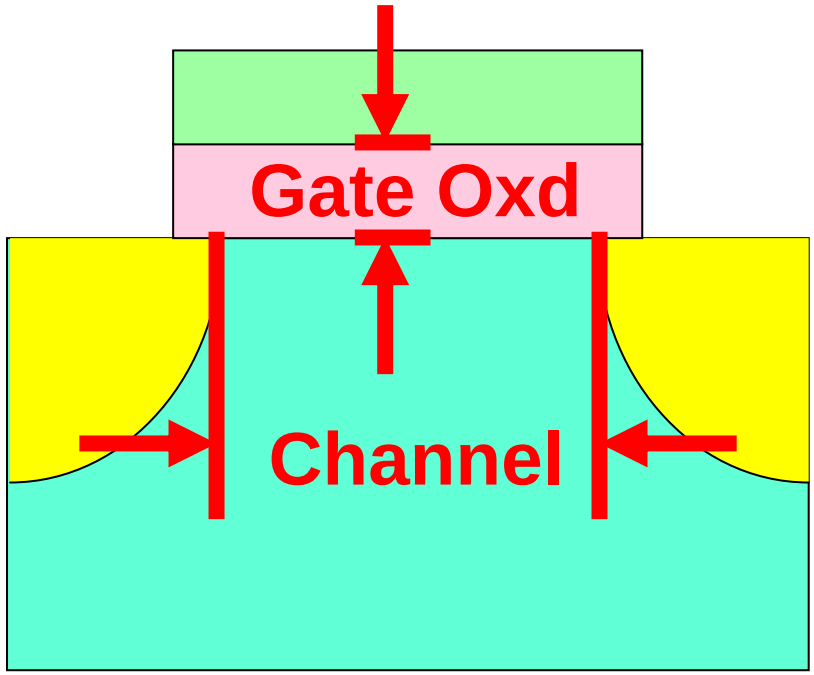
3 nm



Downsizing limit!

Channel length

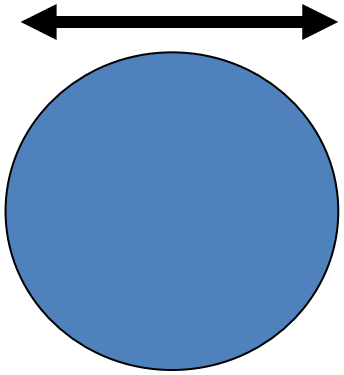
Gate oxide thickness



Prediction now!

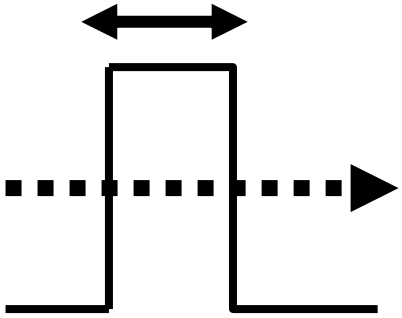
Electron wave length

10 nm



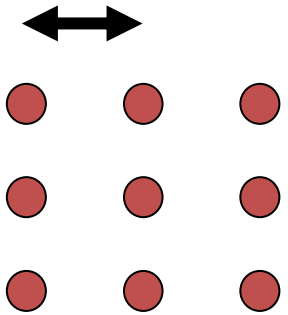
Tunneling distance

3 nm



Atom distance

0.3 nm

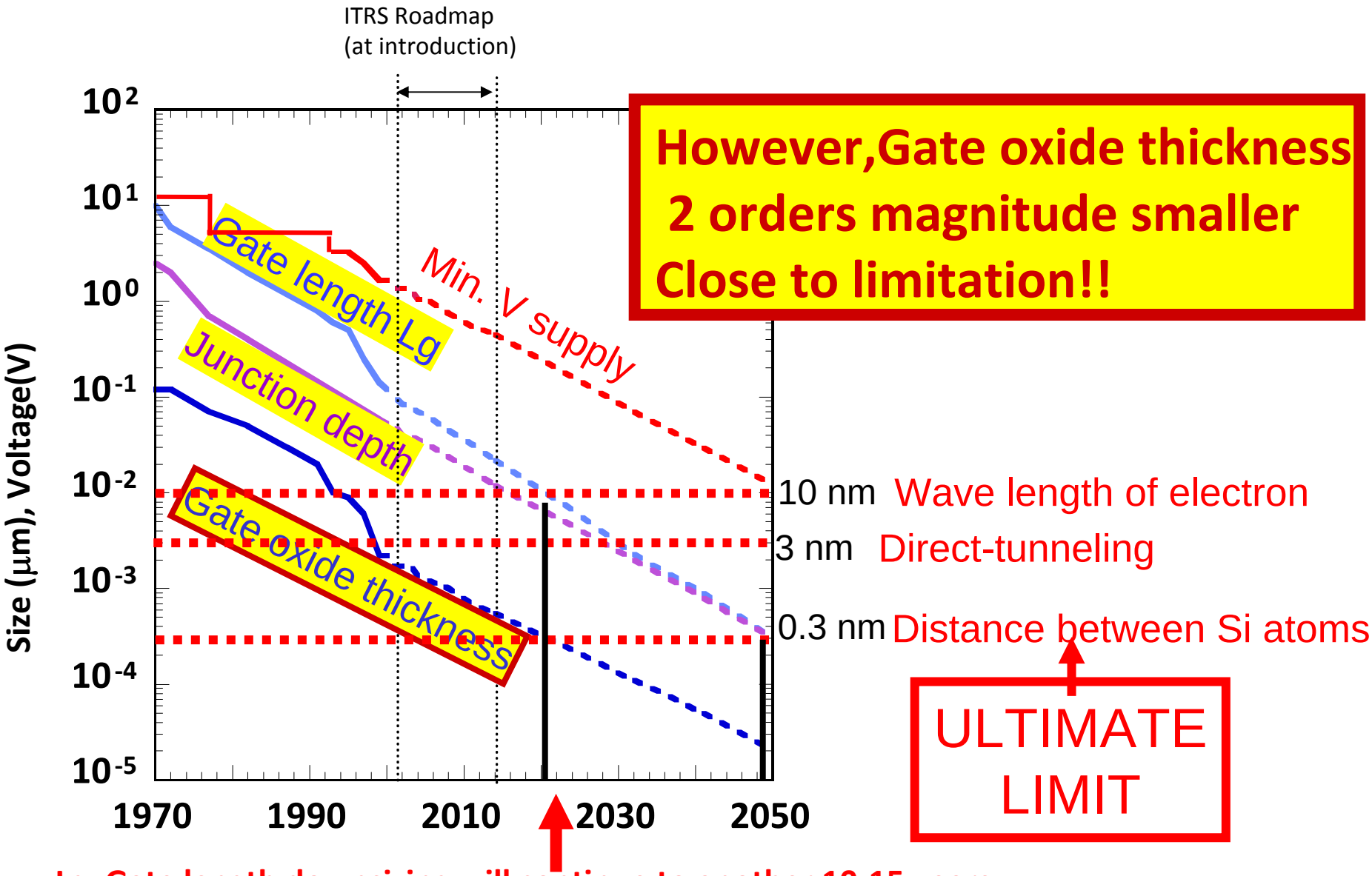


MOSFET operation

Lg = 3 nm?

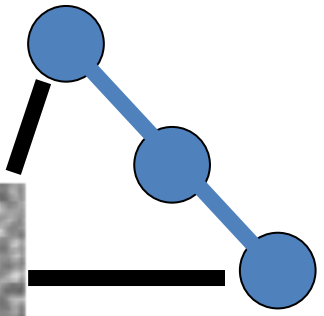
Below this,
no one knows future!

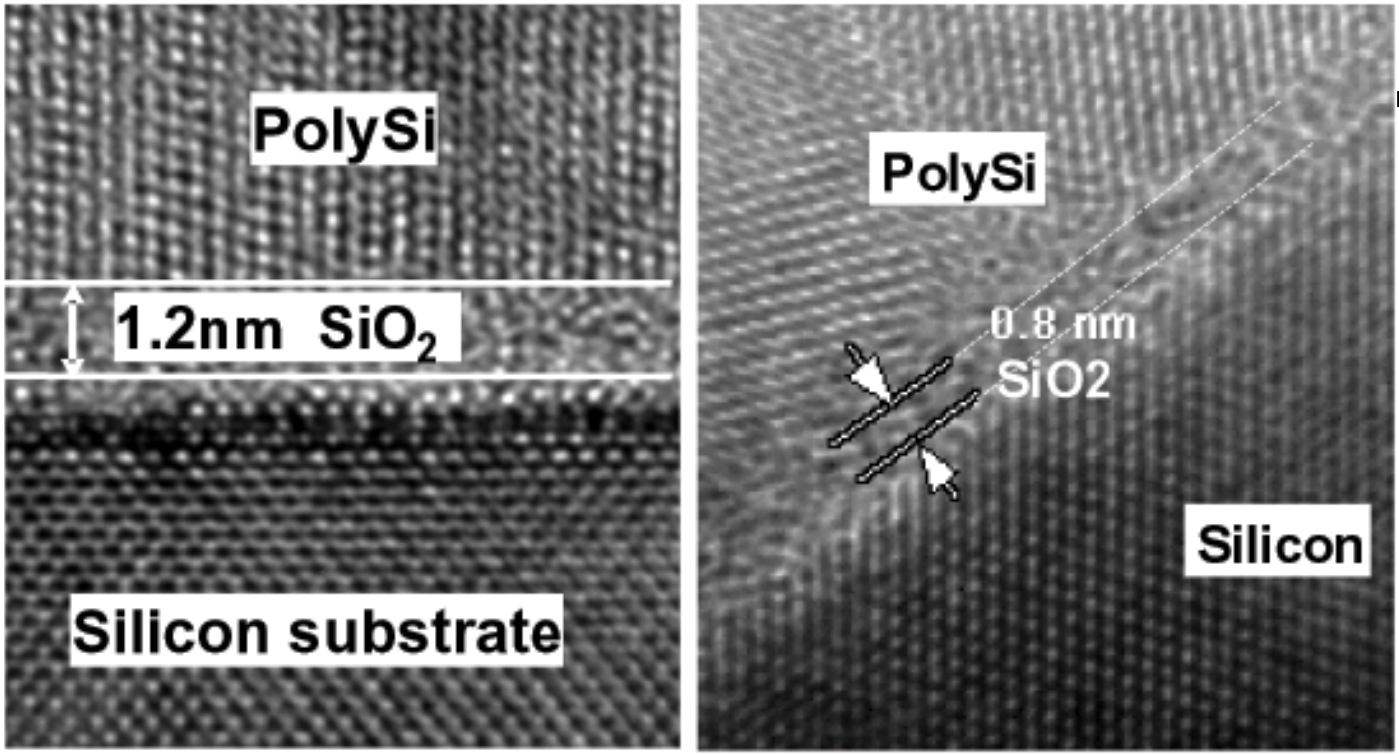
Ultimate limitation



0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!





- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

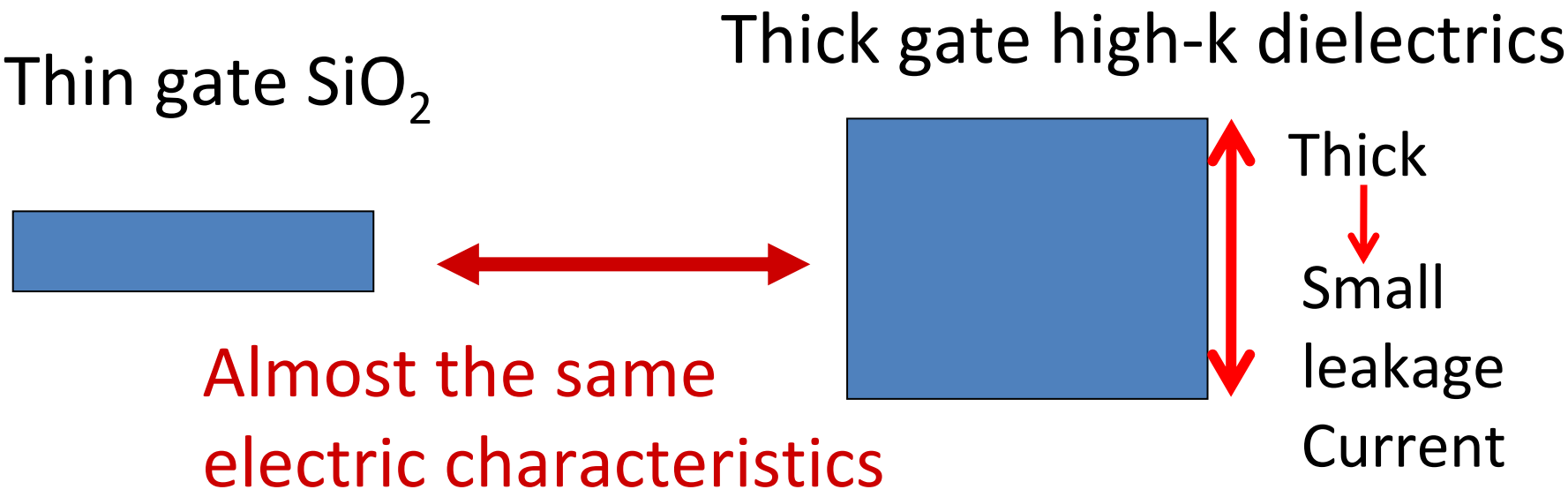
By Robert Chau, IWGI 2003

So, we are now in the limitation of downsizing?

Do you believe this or do not?

There is a solution! K: Dielectric Constant

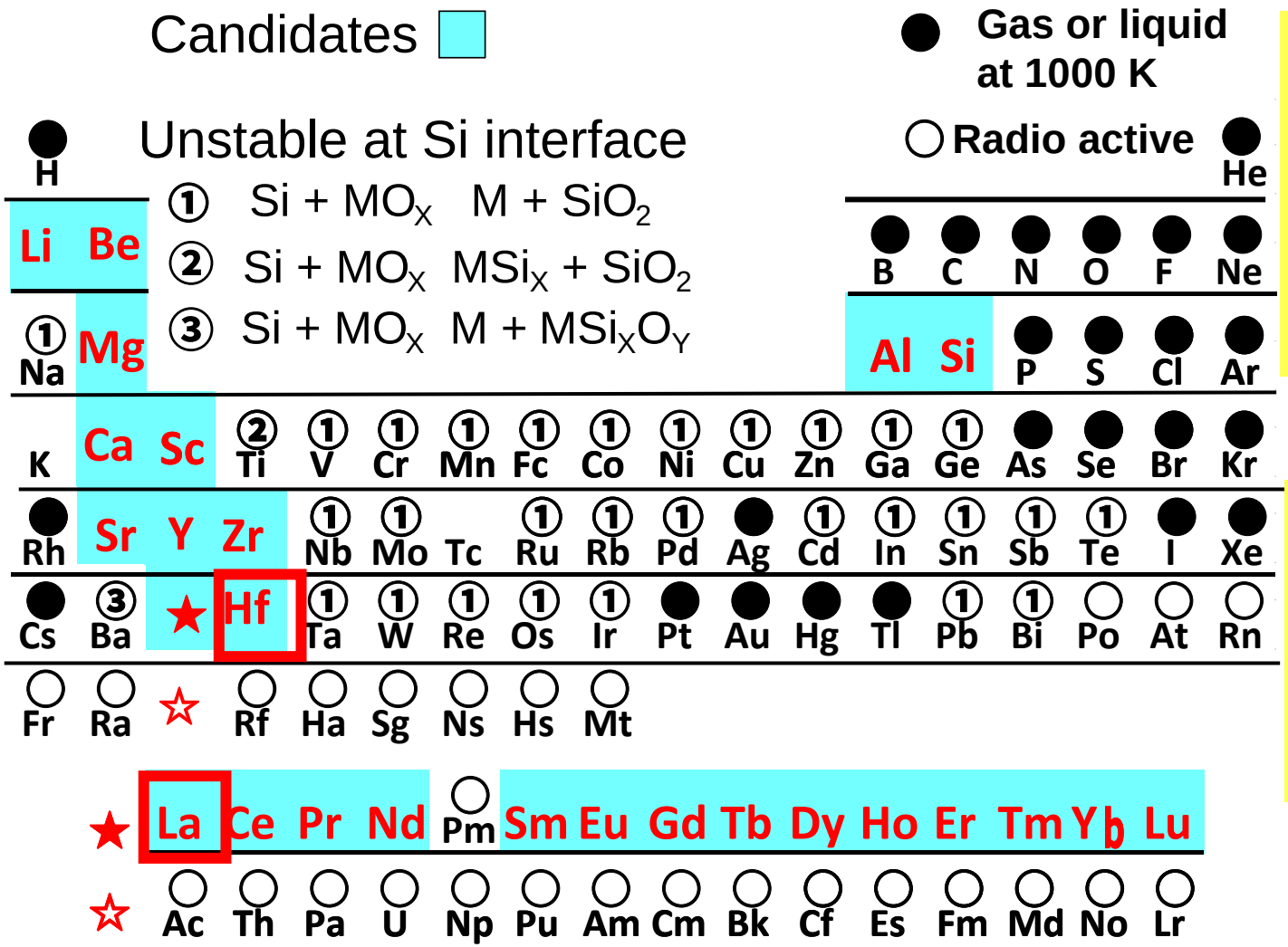
To use high-k dielectrics



However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

Choice of High-k elements for oxide

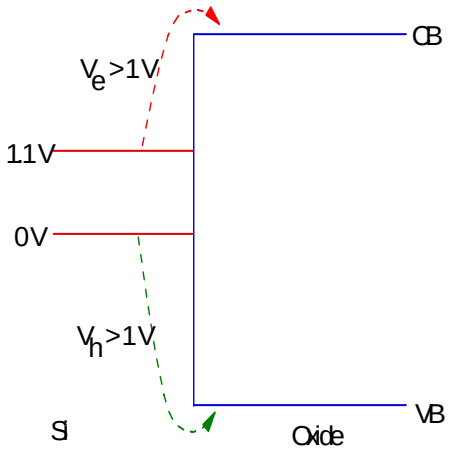


HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

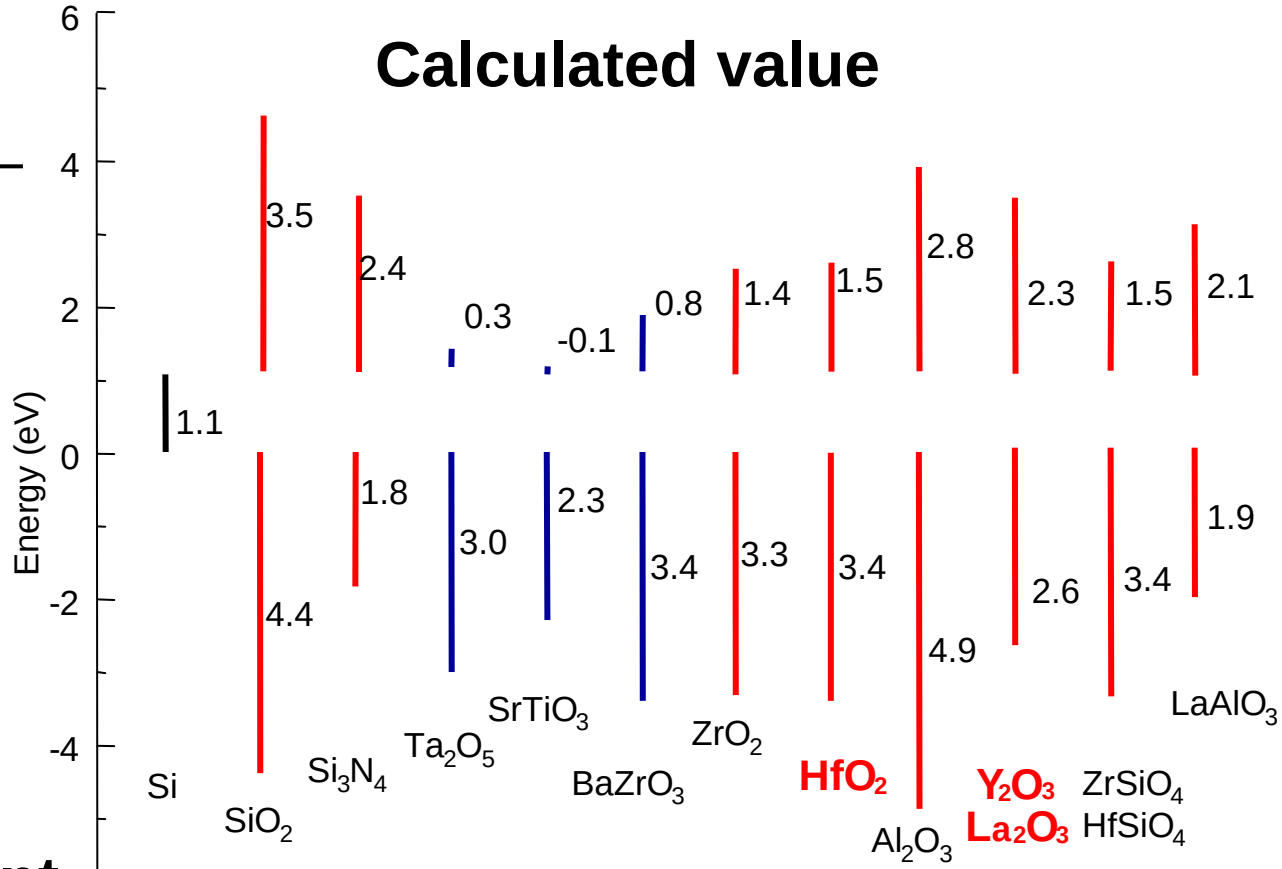
La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

Band Offsets



Dielectric constant



J Robertson, J Vac Sci Technol B **18** 1785 (2000)

SiO2; 4
Si3N4: ~ 7
Al2O3: ~ 9

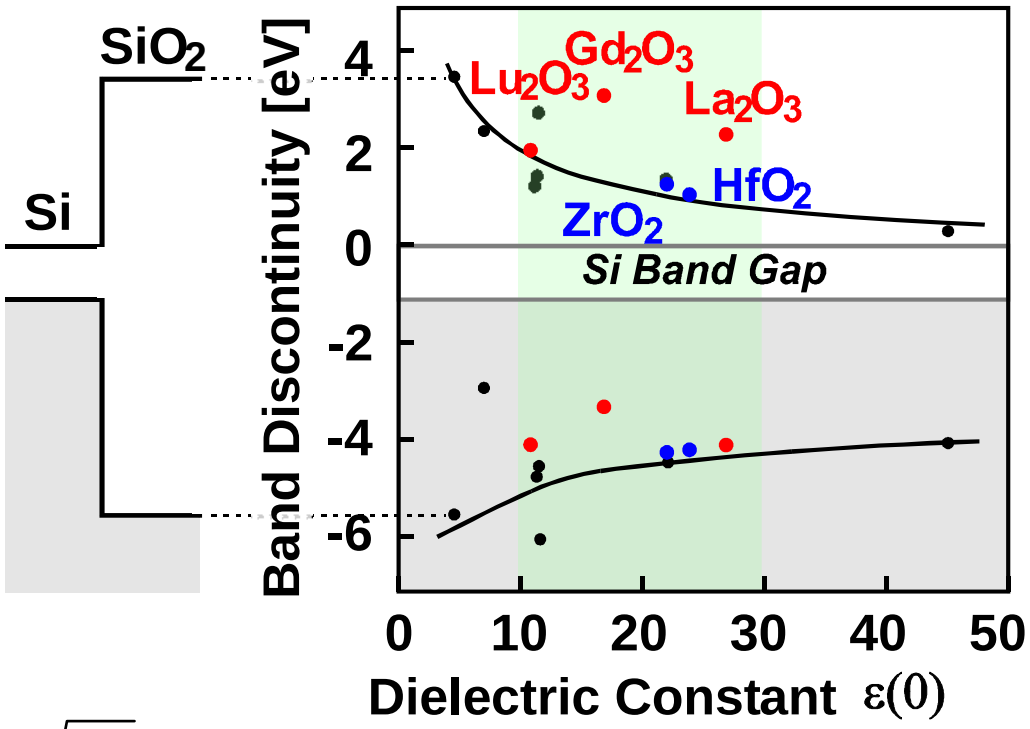
Y2O3; ~10
Gd2O3: ~10

HfO2; ~23
La2O3: ~27

HfO2 was chosen for the 1st generation
La2O3 is more difficult material to treat

Dielectric constant value vs. Band offset (Measured)

SiO_2	3.9	$NdAlO_3$	22.5
Al_xSi_yOz		$PrAlO_3$	25
$(Ba,Sr)TiO_3$	200-300	Si_3N_4	7
$BeAl_2O4$	8.3-9.43	$SmAlO_3$	19
CeO_2	16.6-26	$SrTiO_3$	150-250
$CeHfO_4$	10-20	Ta_2O_5	25-24
$CoTiO_3/Si_3N_4$		Ta_2O_5-TiO_2	
$EuAlO_3$	22.5	TiO_2	86-95
HfO_2	26-30	TiO_2/Si_3N_4	
Hf silicate	11	Y_2O_3	8-11.6
La_2O_3	20.8	$Y_xSi_yO_z$	
$LaScO_3$	30	ZrO_2	22.2-28
La_2SiO_5		Zr-Al-O	
$MgAl_2O_4$		Zr silicate	
		$(Zr,Sn)TiO_4$	40-60



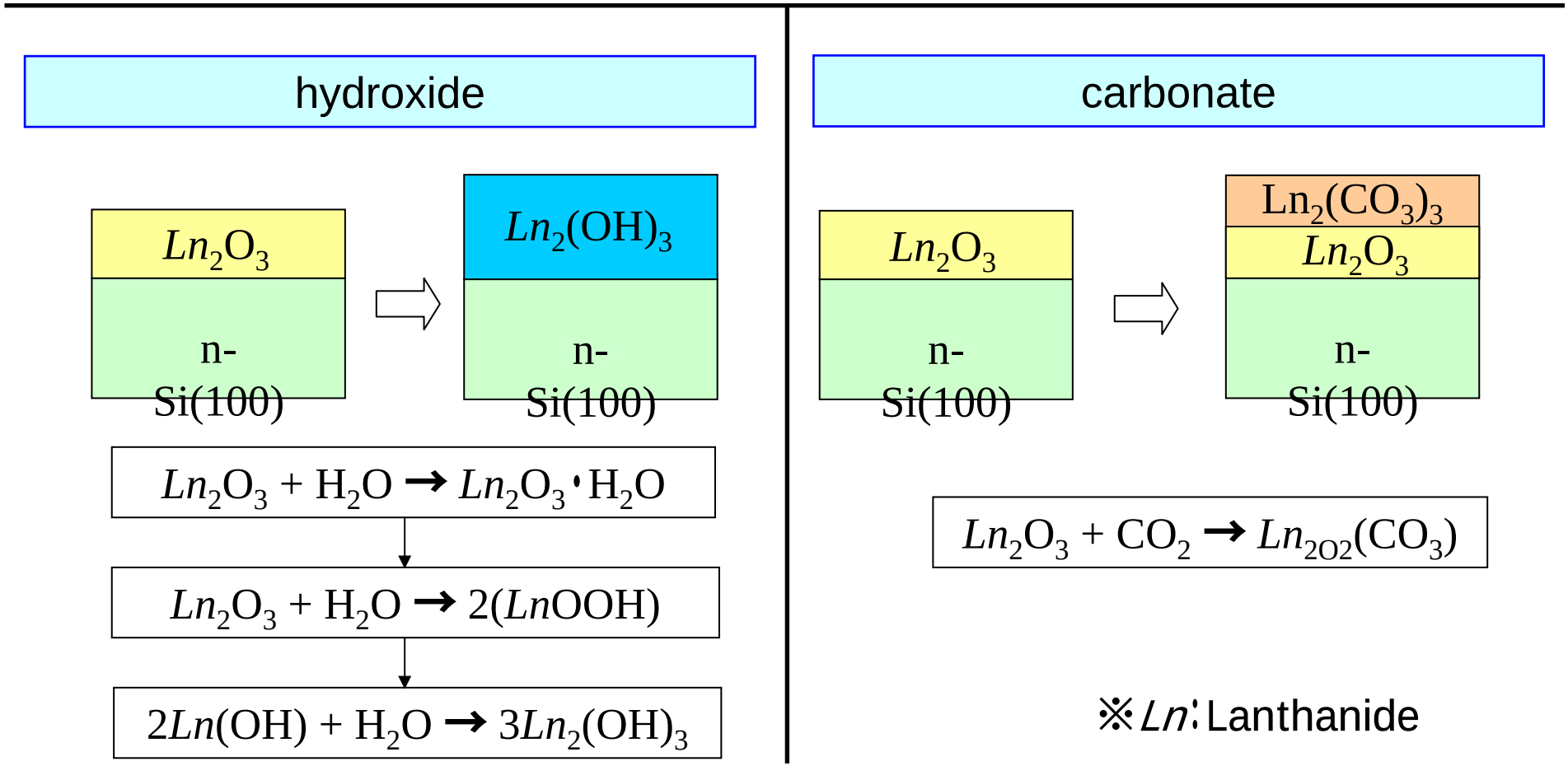
$\sqrt{\phi_B} * k$: Figure of Merit of High-k

C.A. Billmann et al.,, MRS Spring Symp., 1999,
R.D.Shannon, J. Appl. Phys., 73, 348, 1993
S. De Gebdt, IEDM Short Coyuse, 2004

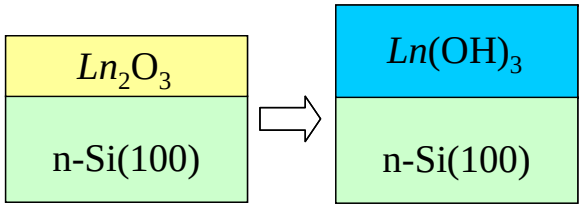
T. Hattori, INFOS , 2003

Absorption of moisture and CO_2

The oxides become hydroxide and carbonate in H_2O and CO_2 ambient.



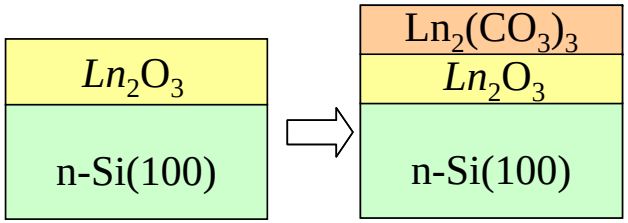
Hygroscopic Properties of La_2O_3



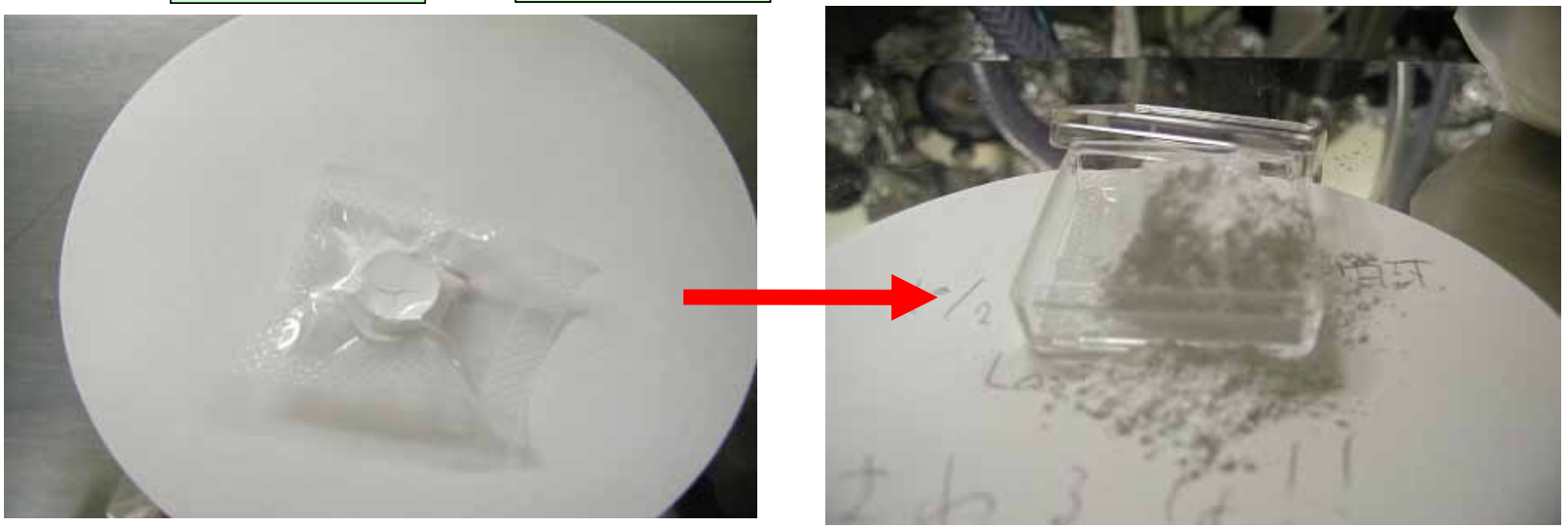
$$Ln_2O_3 + H_2O \rightarrow Ln_2O_3 \cdot H_2O$$

$$Ln_2O_3 \cdot H_2O \rightarrow 2(LnOOH)$$

$$LnOOH + H_2O \rightarrow Ln(OH)_3$$



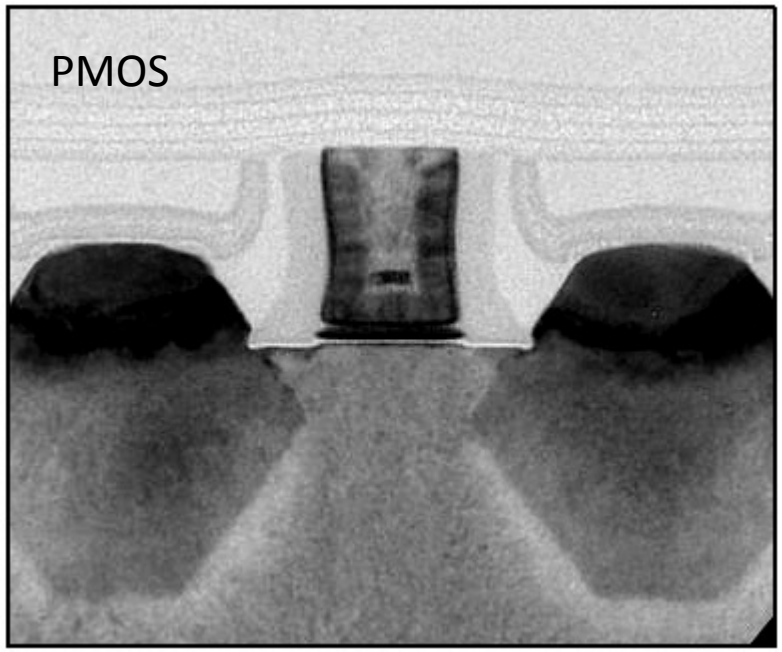
$$Ln_2O_3 + 2CO_2 \rightarrow Ln_2(CO_3)_3$$

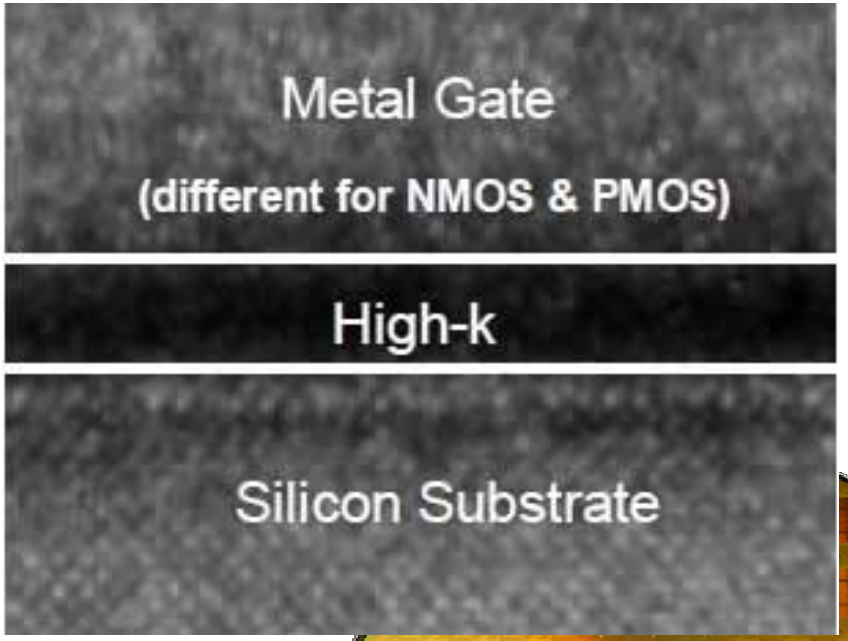


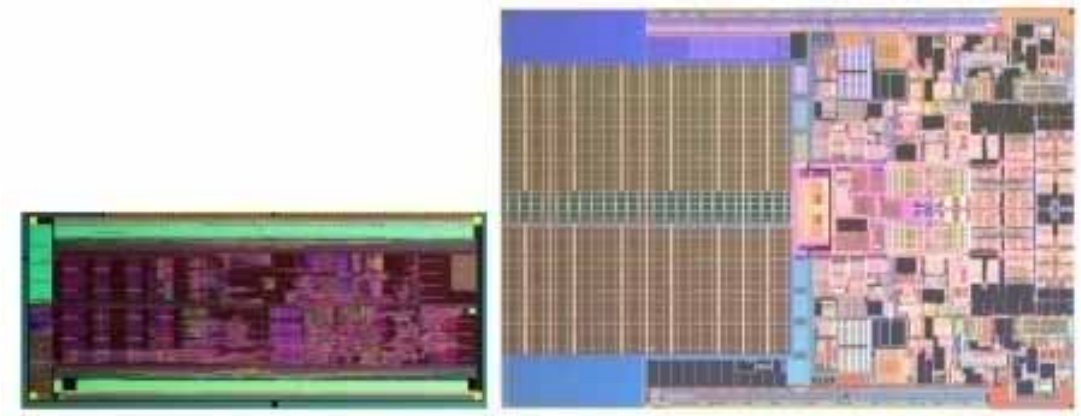
After 30 hours in clean room (temperature & humidity controlled)

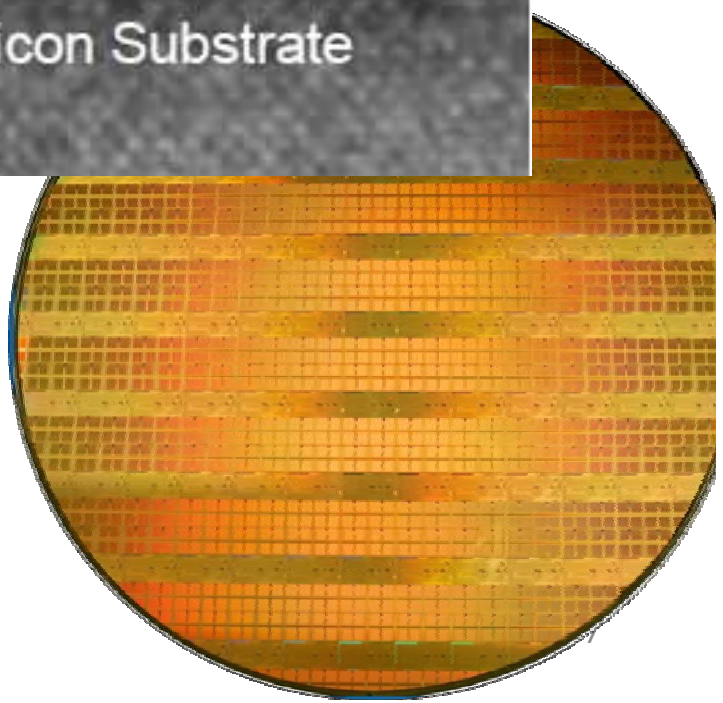
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness

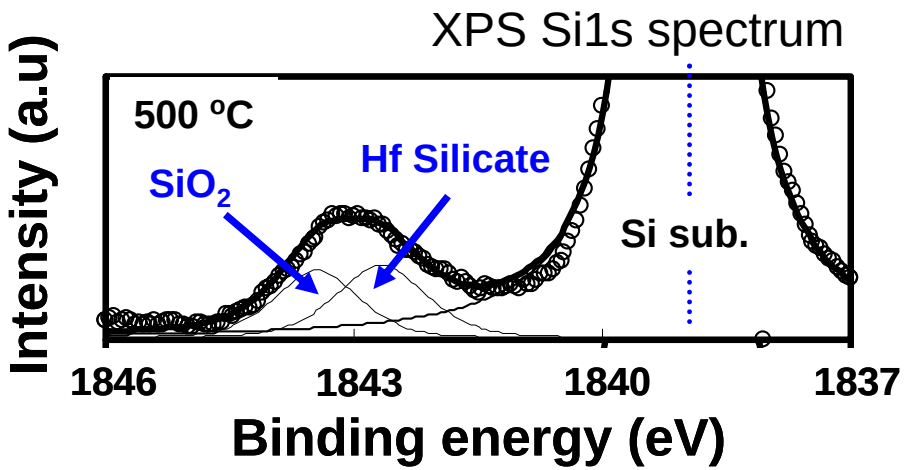


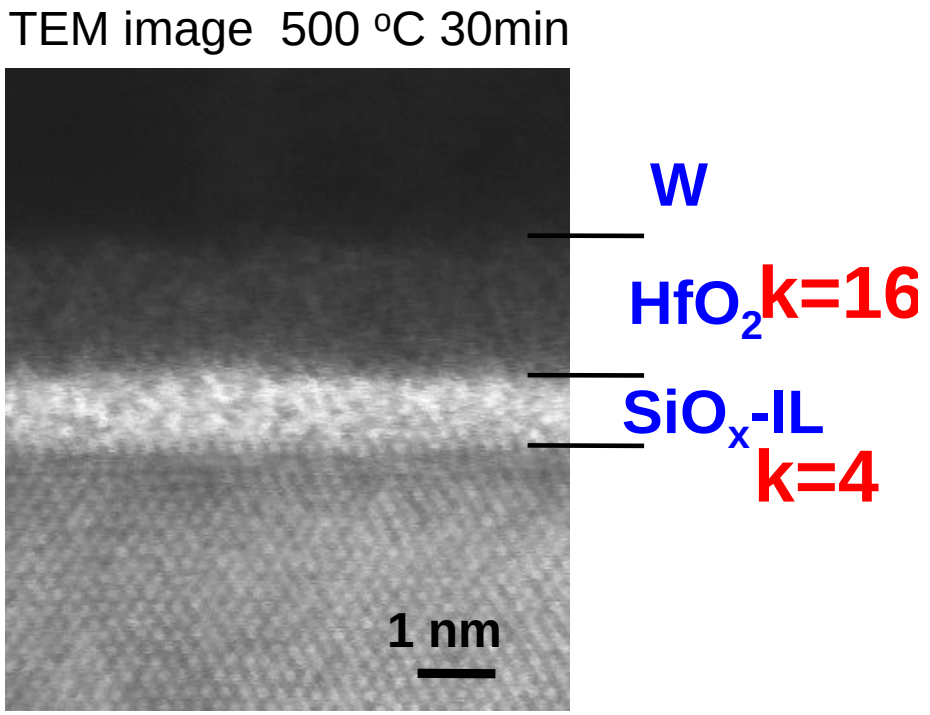






SiO_x-IL growth at HfO_2/Si Interface





Phase separator

$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

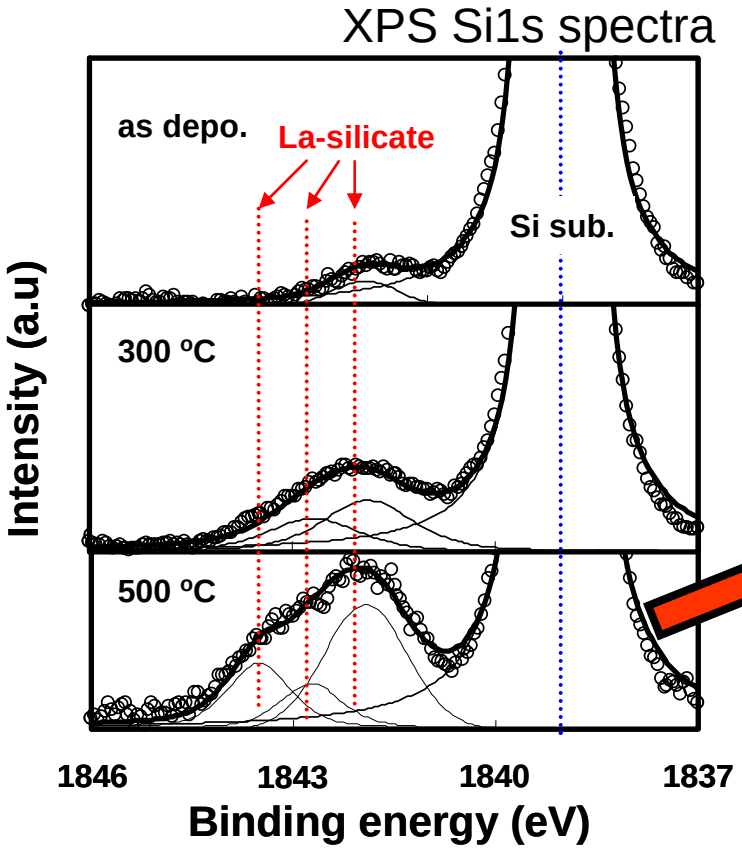
D.J.Lichtenwalner, Tans. ECS 11, 319

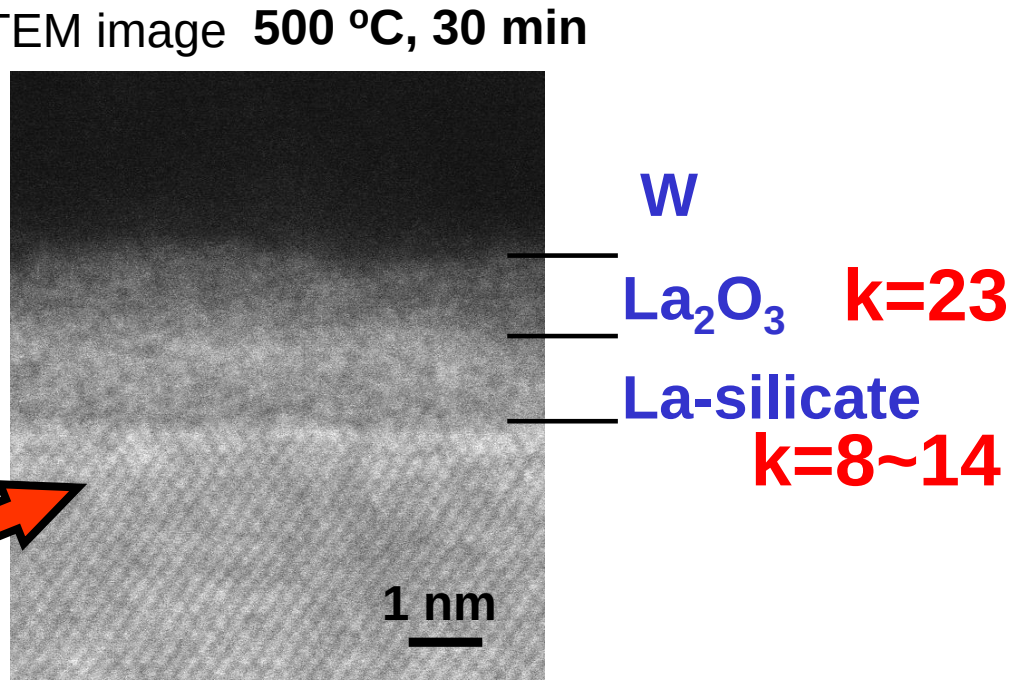
SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

La-Silicate Reaction at La_2O_3/Si

Direct contact high-k/Si is possible

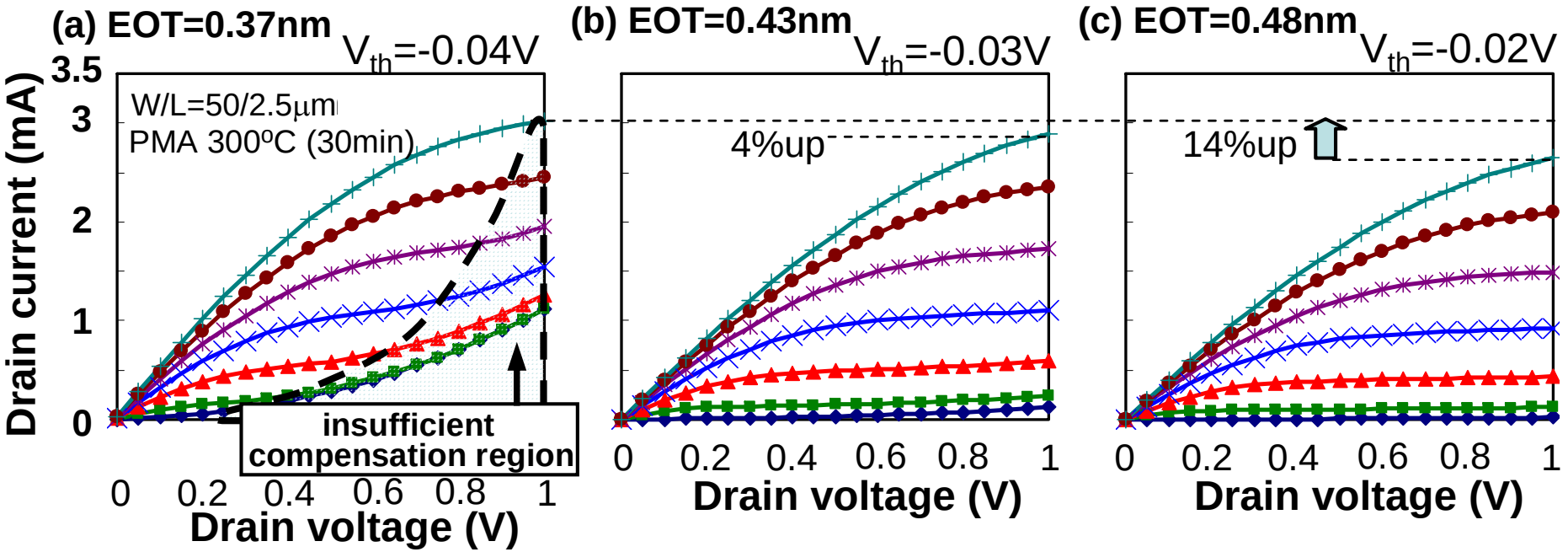




$La_2O_3 + Si + nO_2$
→ La_2SiO_5, $La_2Si_2O_7$,
$La_{9.33}Si_6O_{26}$, $La_{10}(SiO_4)_6O_3$, etc.

La_2O_3 can achieve direct contact of high-k/Si

EOT<0.5nm with Gain in Drive Current



14% of I_d increase is observed even at saturation region

EOT below 0.4nm is still useful for scaling

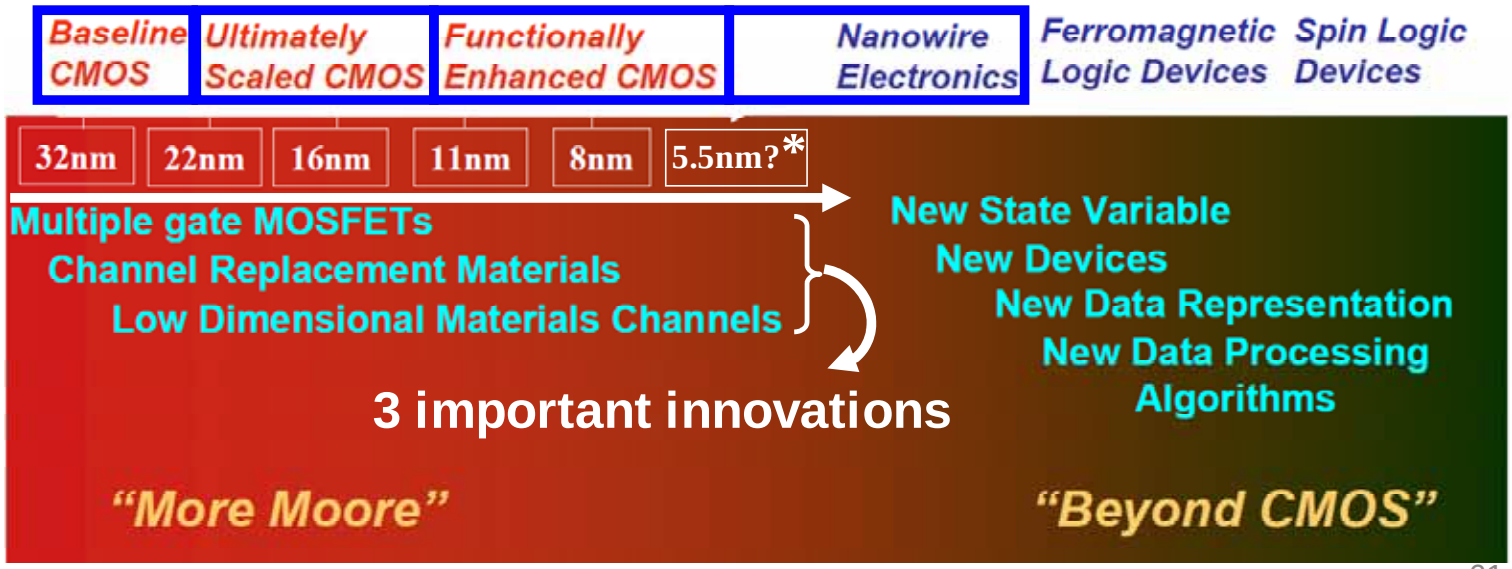
-There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.



ITRS figure edited by Iwai

Source: 2008 ITRS Summer Public Conf.

***5.5nm? was added by Iwai**

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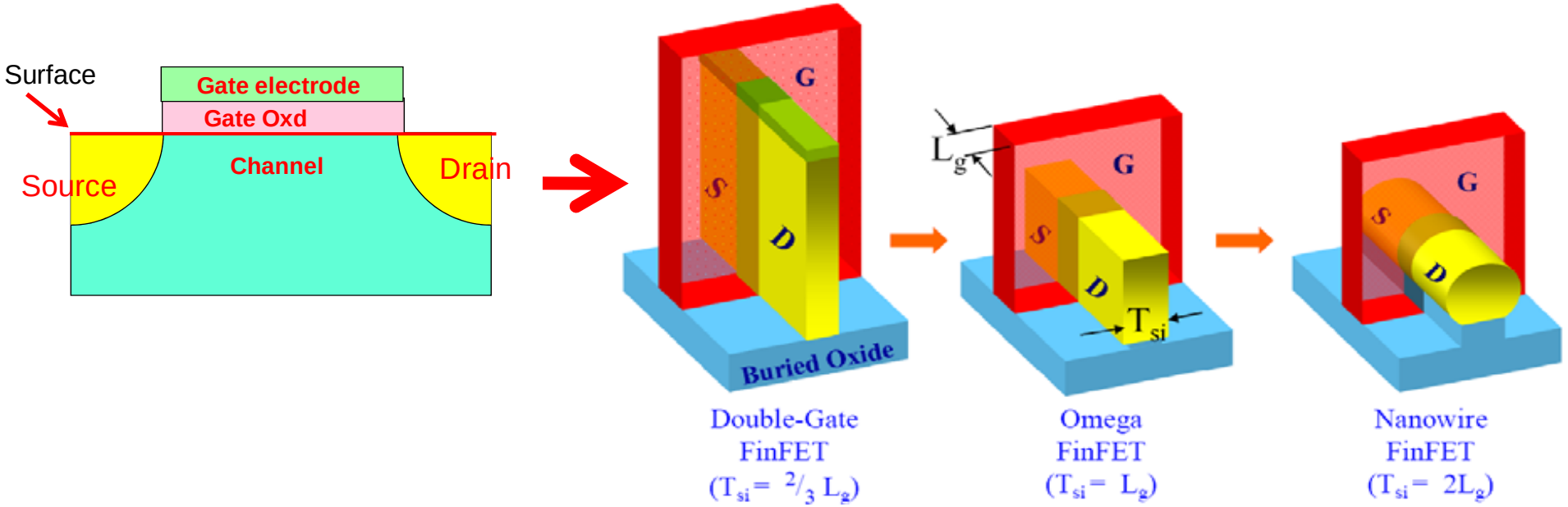
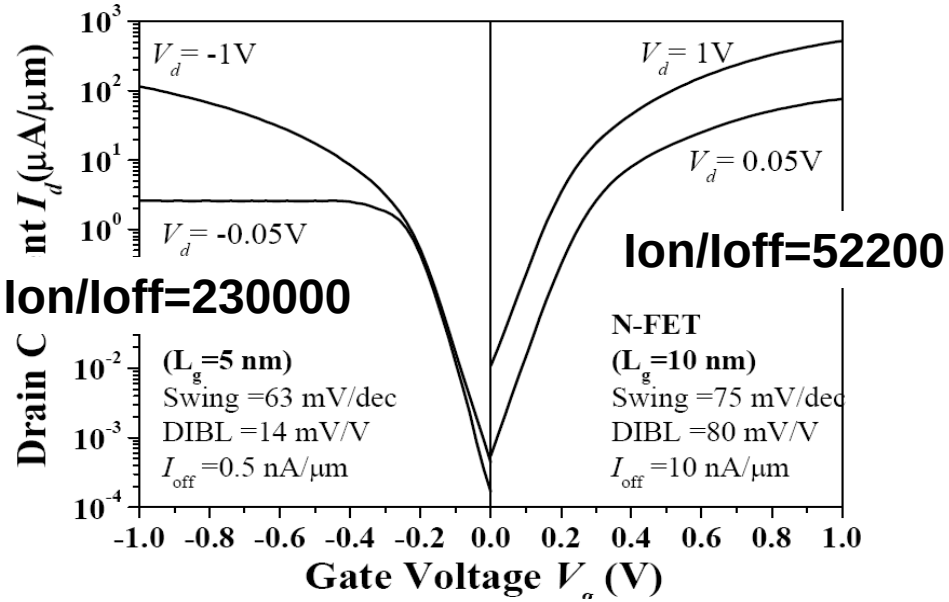
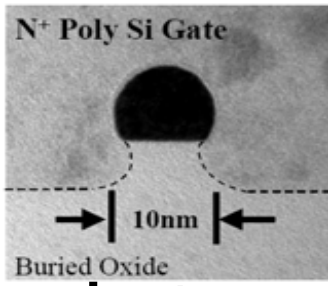
FinFET to Nanowire







Channel conductance is well controlled by Gate even at L=5nm

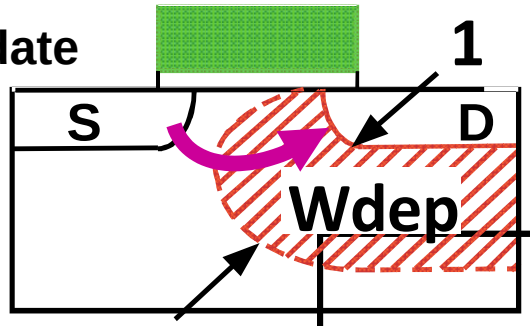
F.-L.Yang, VLSI2004

Si nanowire FET as a strong candidate

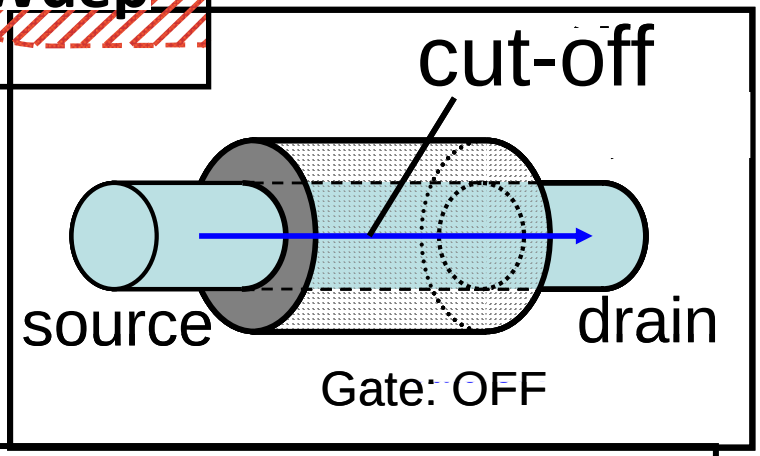
1. Compatibility with
   current CMOS process

2. Good controllability of I_{OFF}

3. High drive current

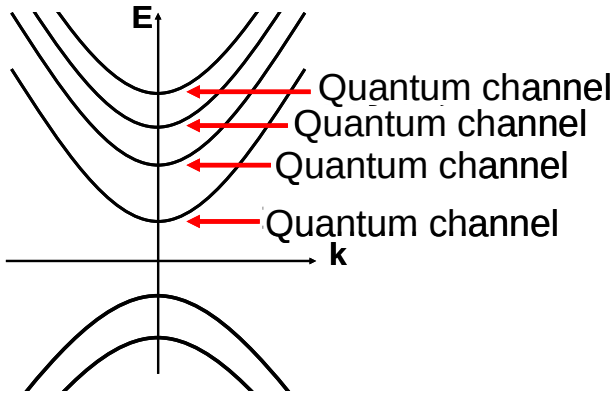


Leakage current

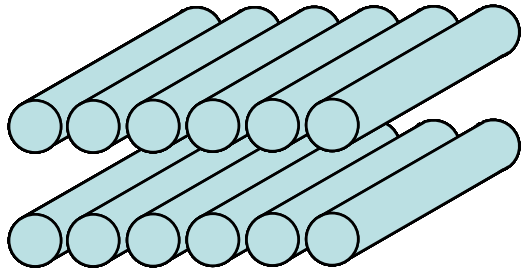


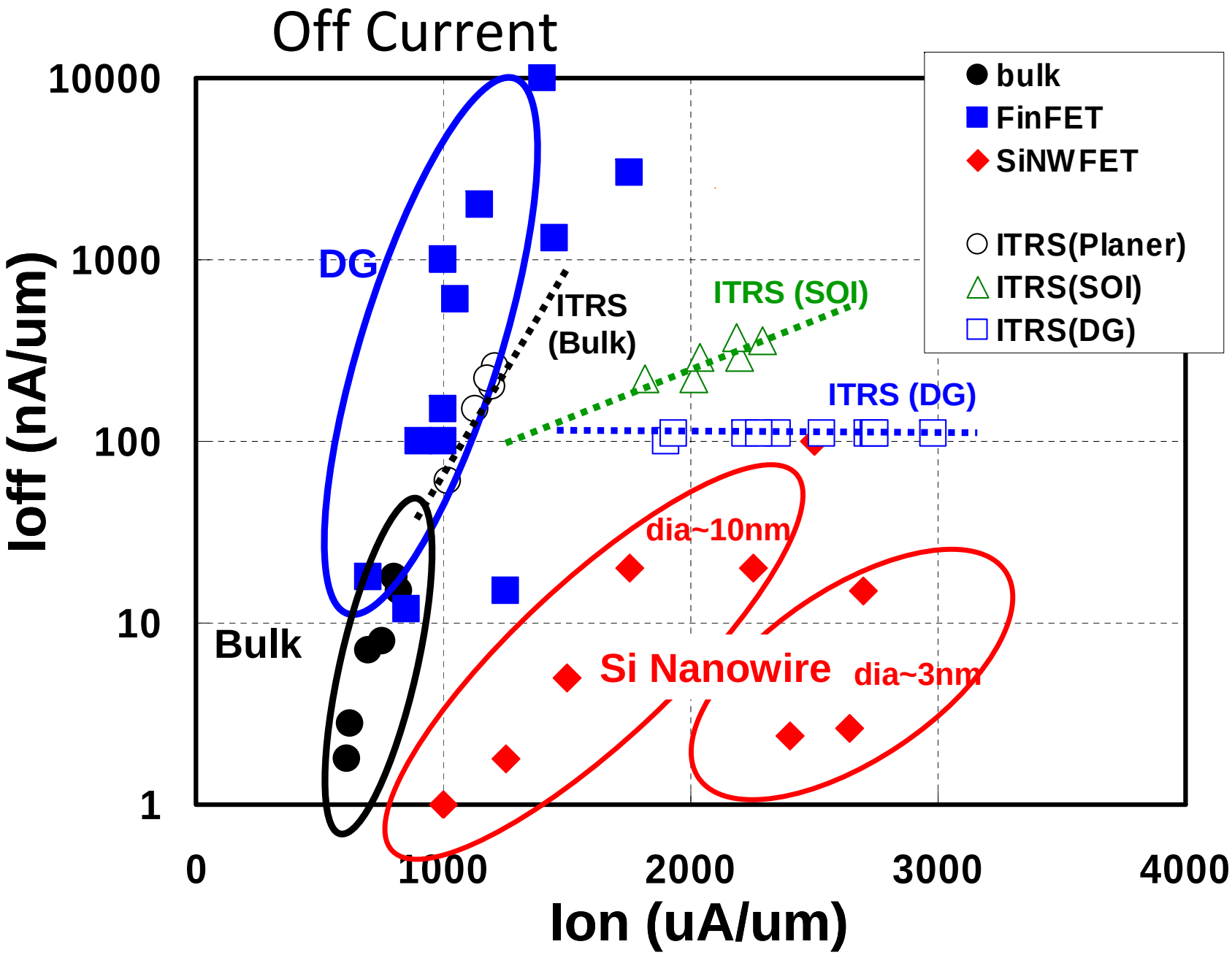
1D ballistic conduction

Multi quantum Channel



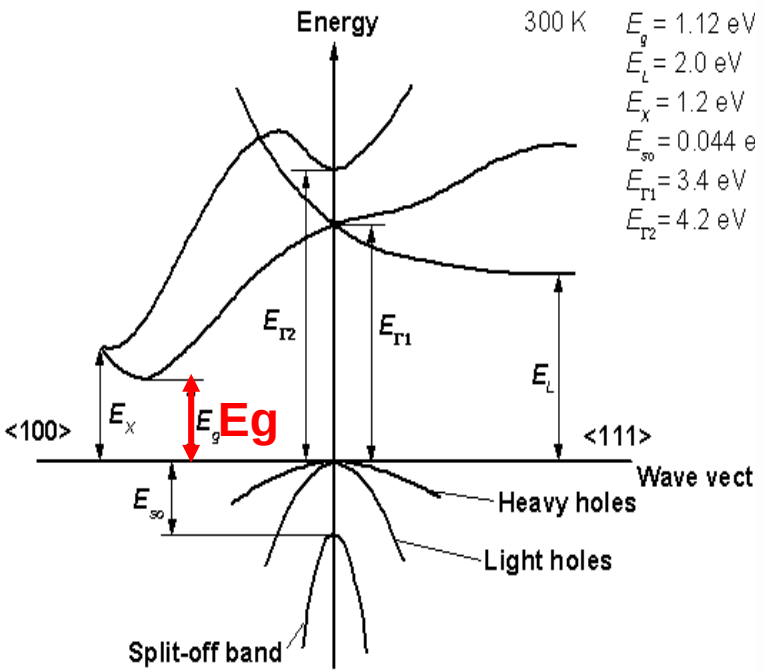
High integration of wires



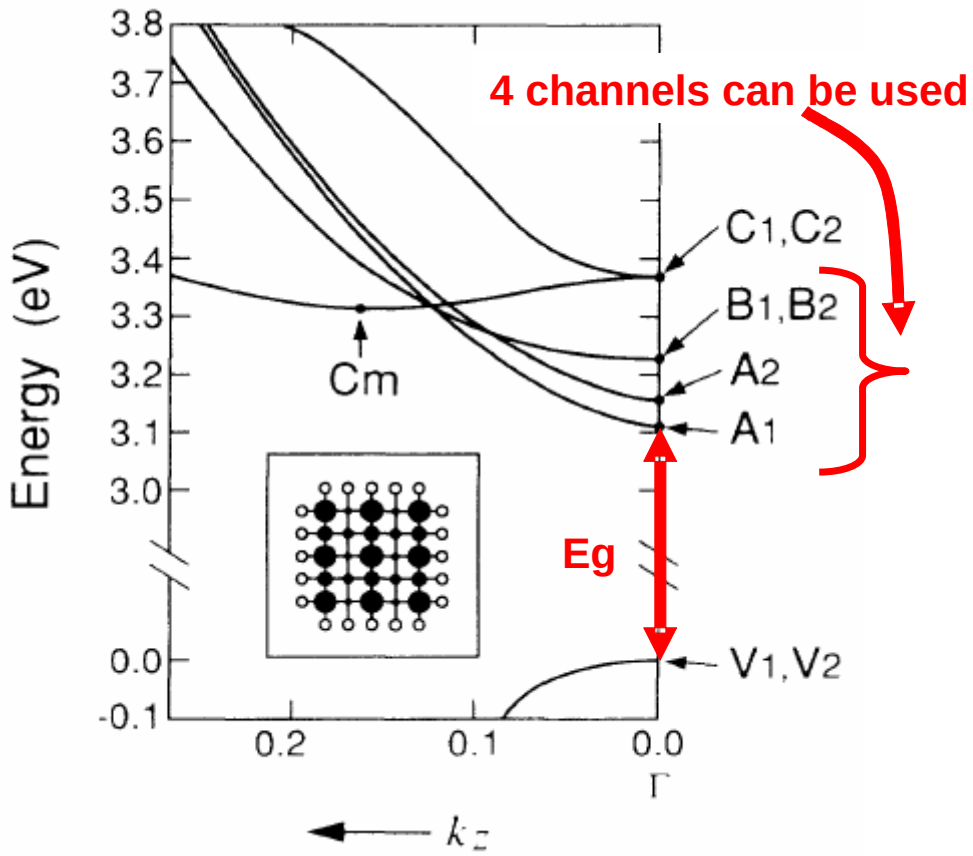

Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



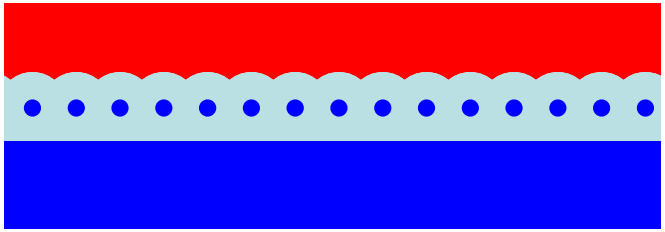
Energy band of Bulk Si



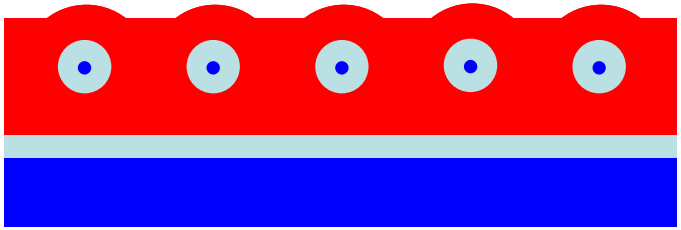
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

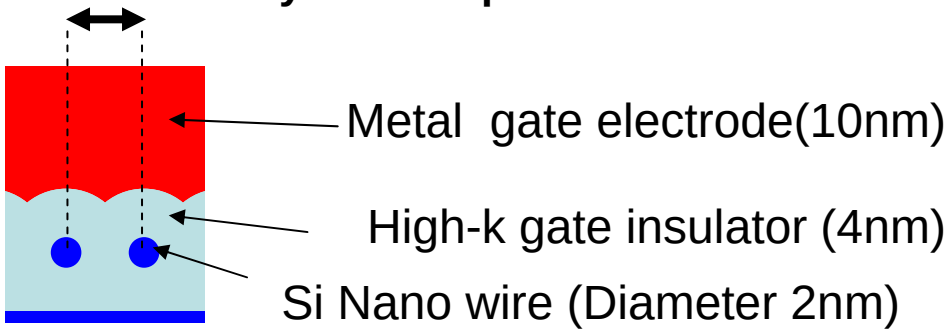
Front gate type MOS 165 wires /μm

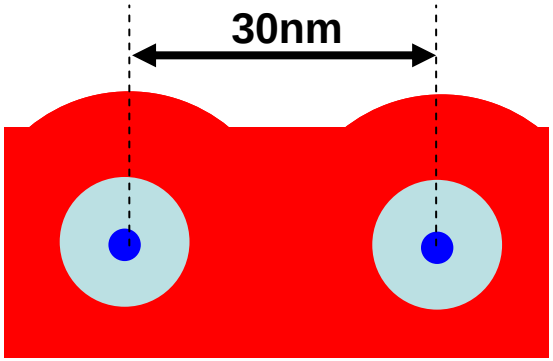


Surrounded gate type MOS 33 wires/μm

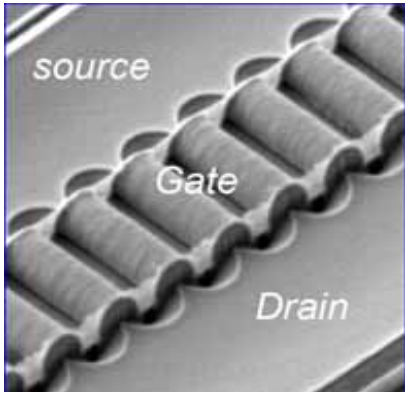


6nm pitch
By nano-imprint method



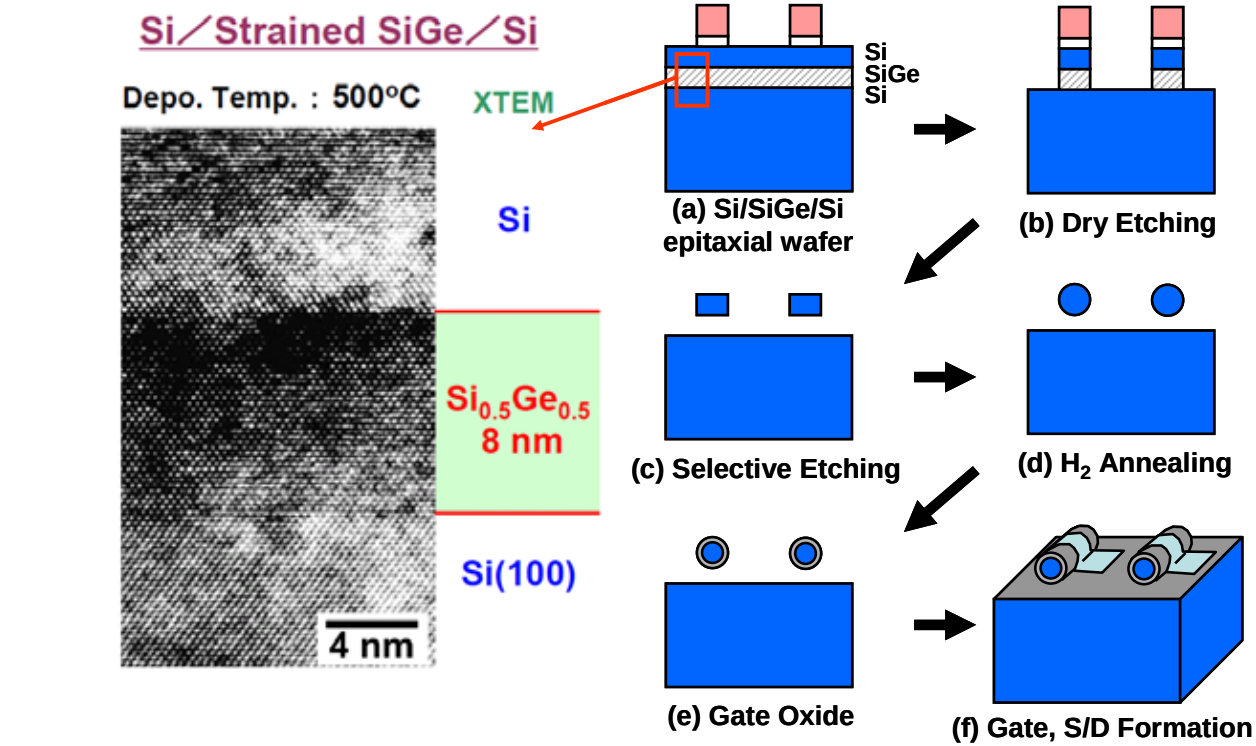


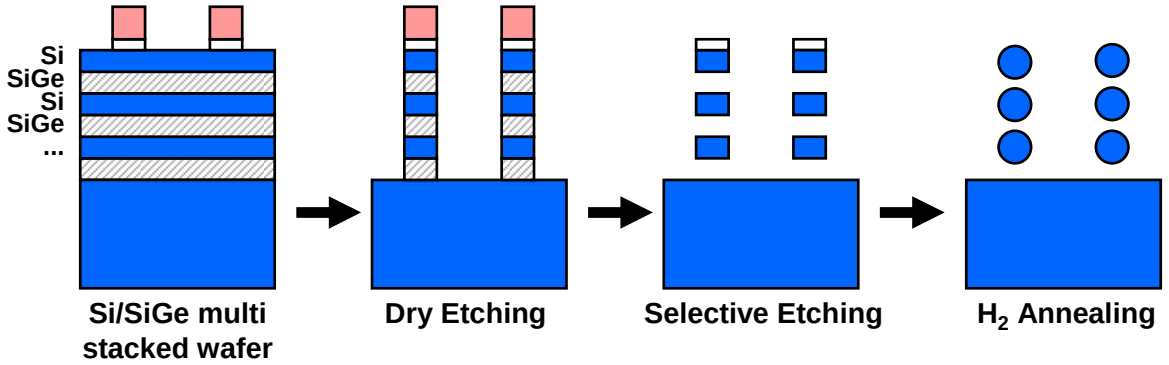
30nm pitch:
EUV lithograpy



Surrounded gate MOS

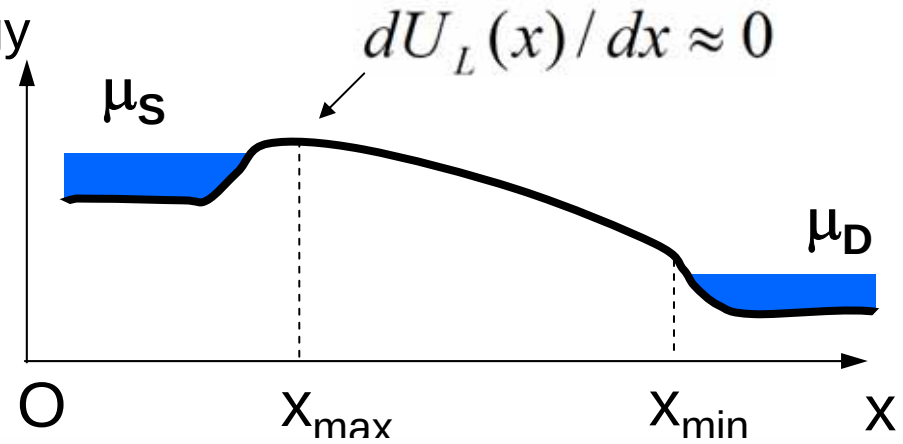
Increase the number of wires towards vertical dimension





Landauer Formalism for Ballistic FET

Potential Energy

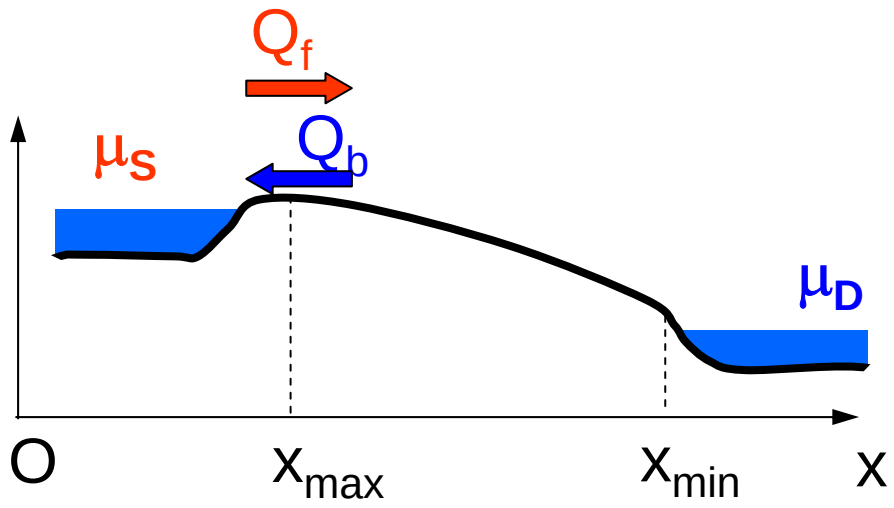


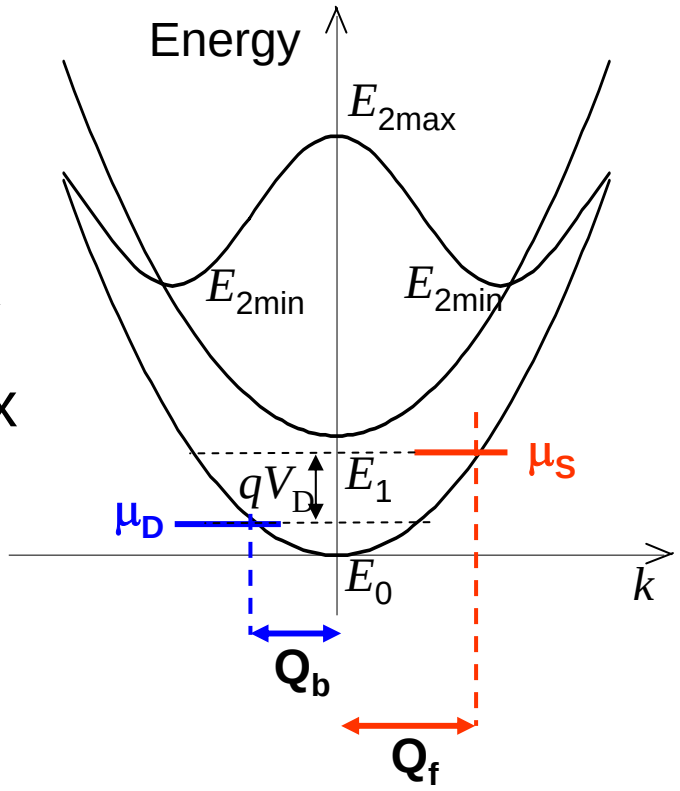
$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D) \right] T_i(E)\, dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0 \left(\frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1+\exp\left[(\mu_S - E_{i0})/k_B T \right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T \right]} \right\}$$

Carrier Density obtained from E-k Band

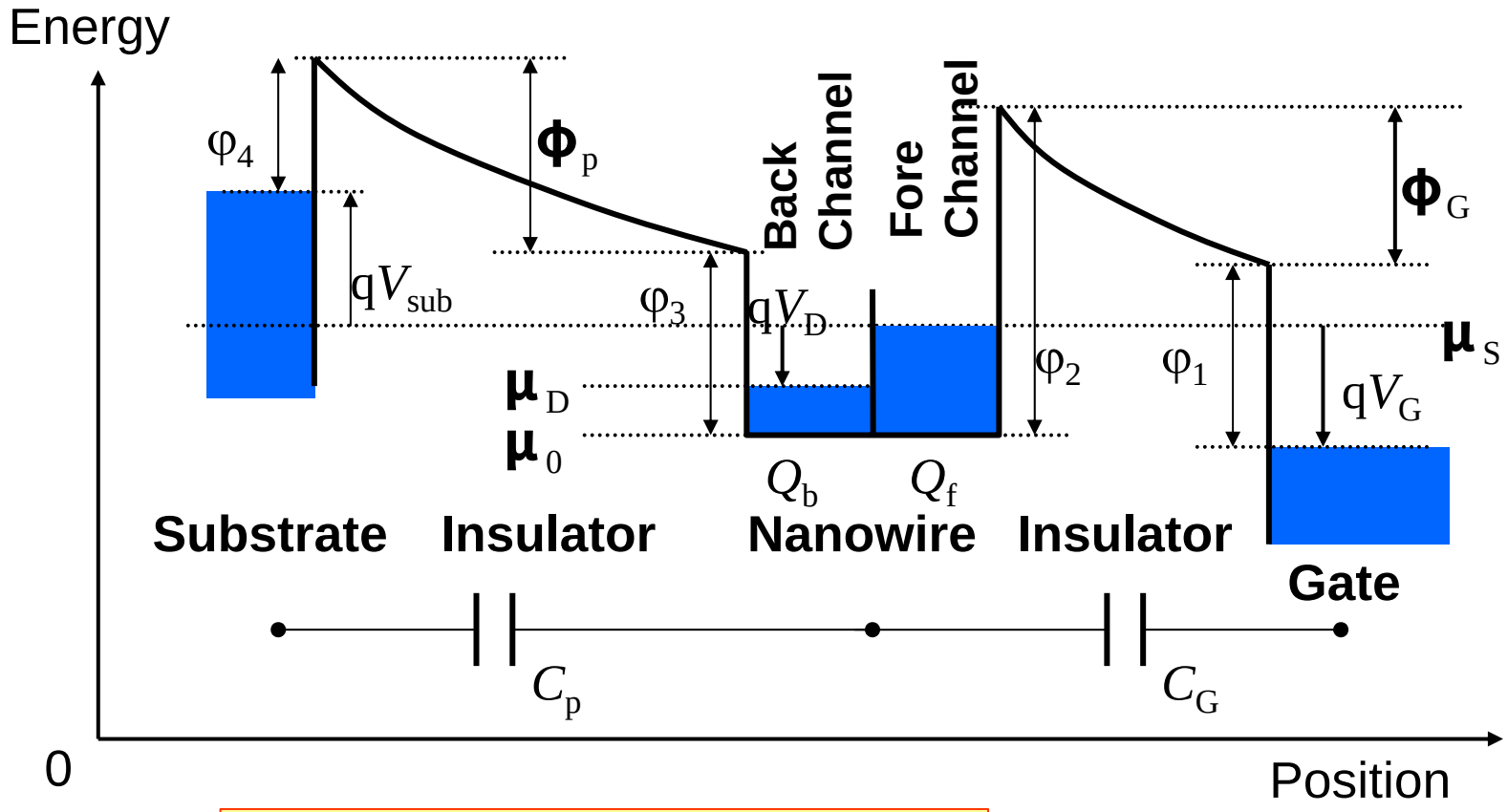




$$|Q| = |Q_f| + |Q_b|$$

$$= \frac{q}{\pi} \sum_i g_i \left[\int_{k_{i\min}}^{\infty} \frac{dk}{1+\exp\left\{\frac{E_i(k)-\mu_S}{k_B T}\right\}} + \int_{-\infty}^{k_{i\min}} \frac{dk}{1+\exp\left\{\frac{E_i(k)-\mu_D}{k_B T}\right\}} \right]$$

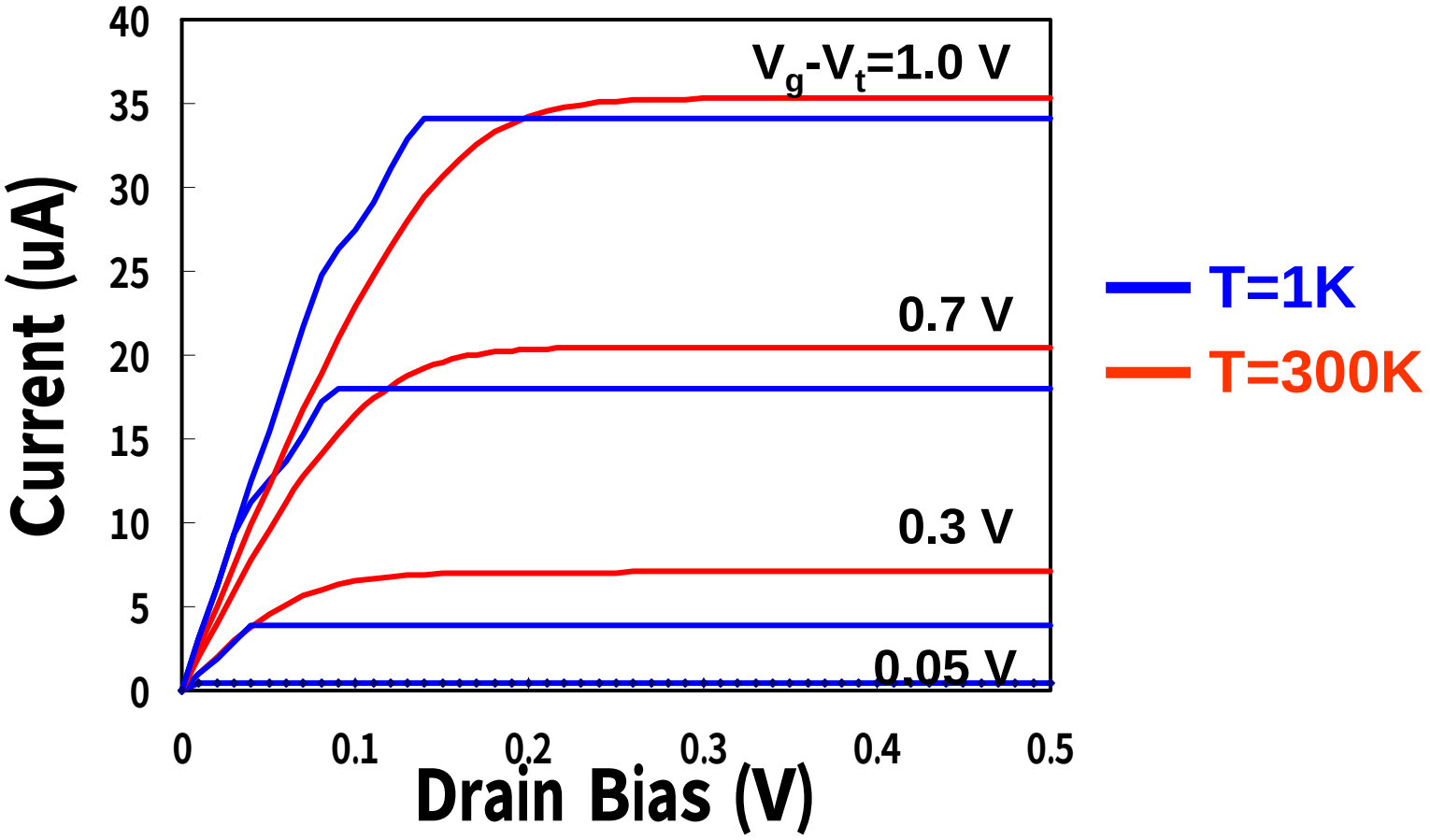
Carrier Density obtained from Band Diagram



$$\frac{|Q|}{C_G} = (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q}$$

$$\alpha = 1 + \frac{C_P}{C_G}$$

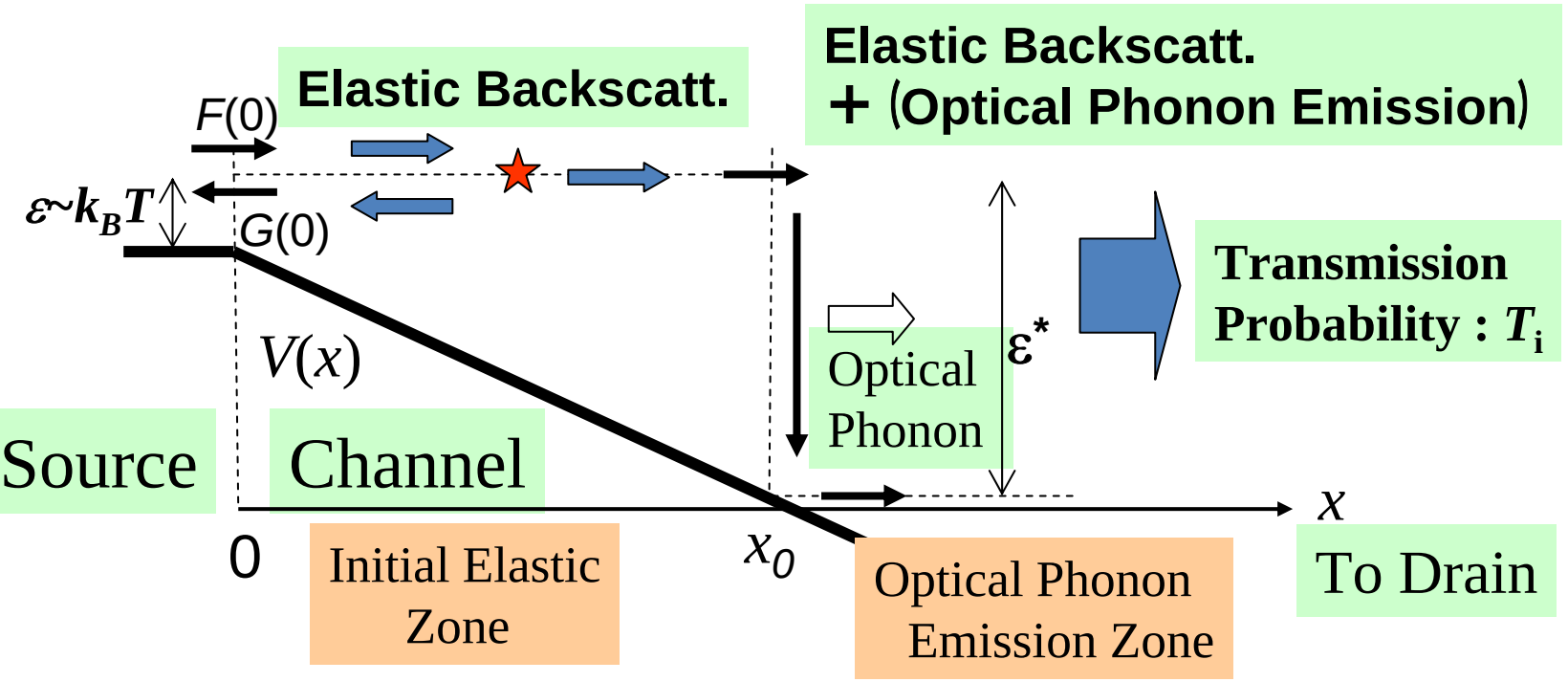
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx. ; Electric Field E



Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{\dfrac{\sqrt{2r+t_{ox}}+\sqrt{t_{ox}}}{\sqrt{2r+t_{ox}}-\sqrt{t_{ox}}}\right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha\frac{\mu_S - \mu_0}{q} = \frac{\left|Q_f + Q_b\right|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\dfrac{r+t_{ox}}{r}\right)}.$$

GAA

(Electrostatics requirement)

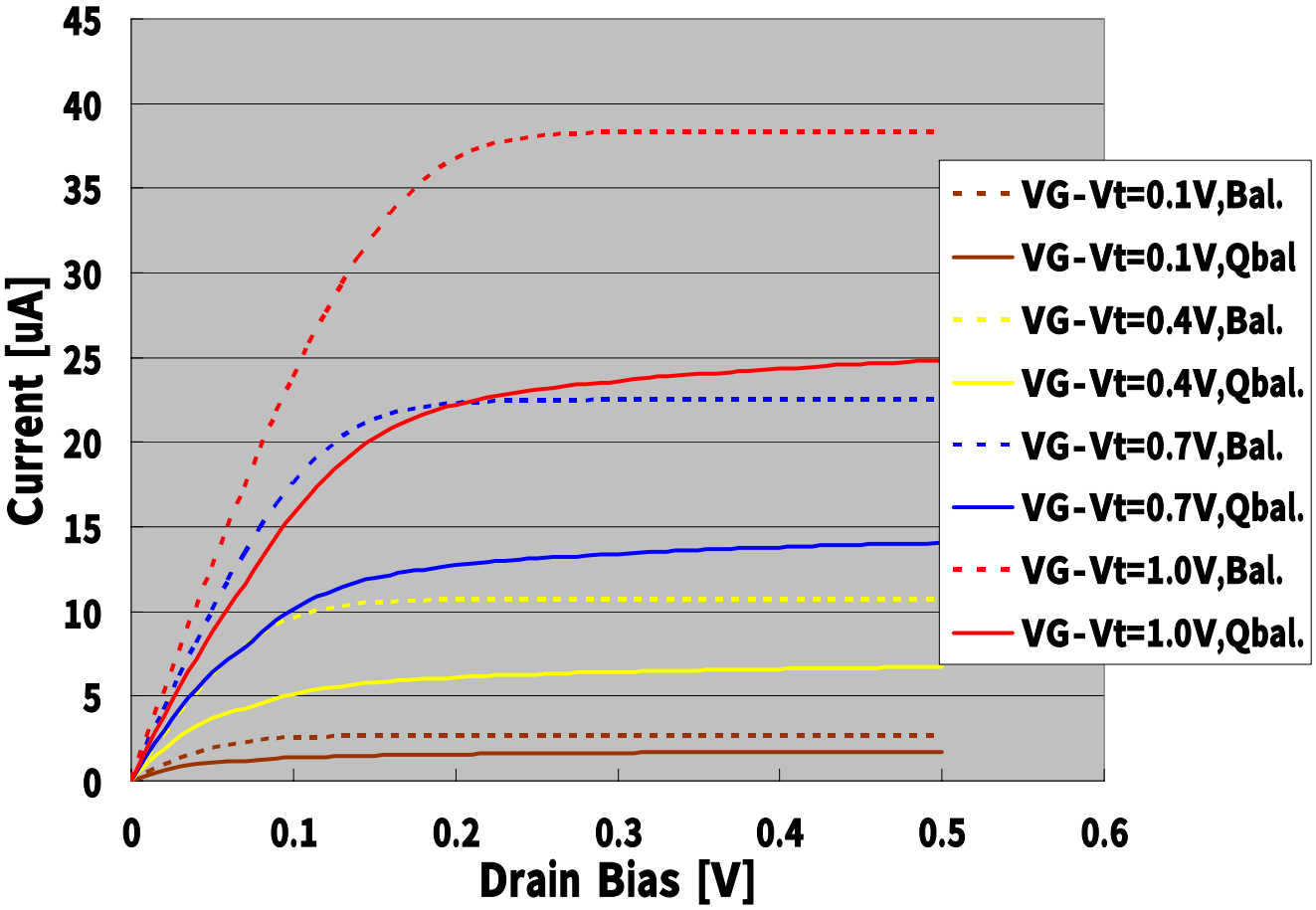
$$\left|Q_f + Q_b\right| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_S}{k_BT}\right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_S}{k_BT}\right\}} - \frac{1}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_D}{k_BT}\right\}} \right\} T_i(\varepsilon_i(k))dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\,qE}{\left(\sqrt{B_0+D_0}+\sqrt{D_0}\right)qE + \sqrt{2mD_0}\,B_0 \ln\left(\dfrac{qEx_0+\varepsilon}{\varepsilon}\right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S-\mu_0)$, $(\mu_D-\mu_0)$, および (Q_f+Q_b)

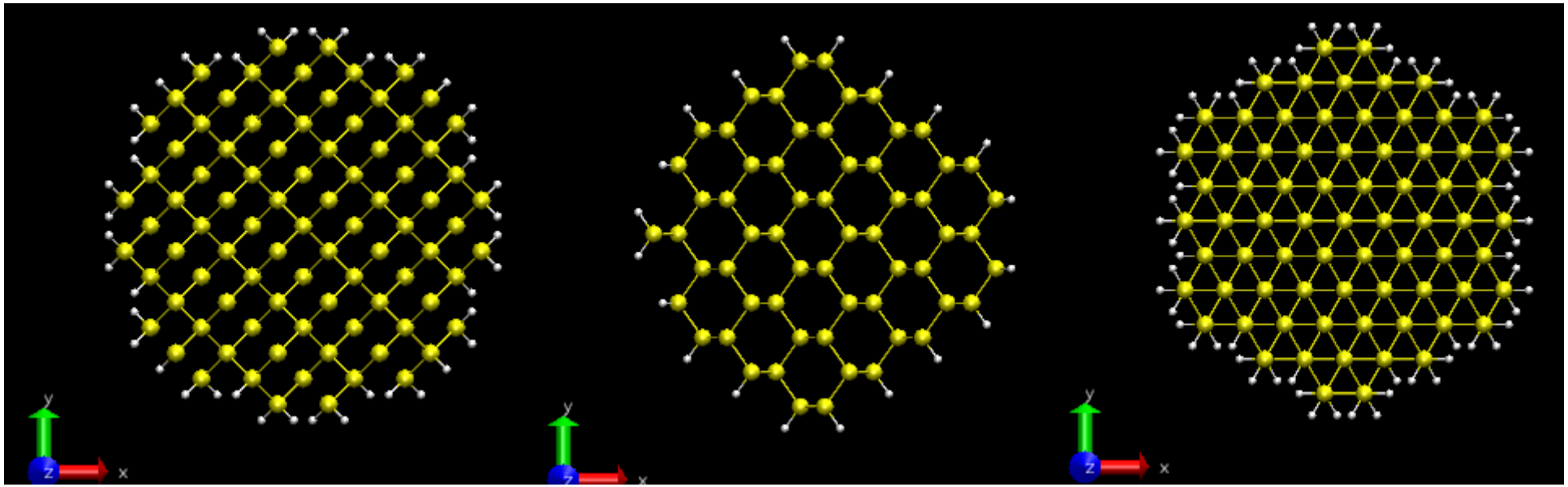
I-V_D Characteritics (RT)



- Electric current 20～25 μA
- No satruration at Large V_D

Cross section of Si NW

First principal calculation, TAPP

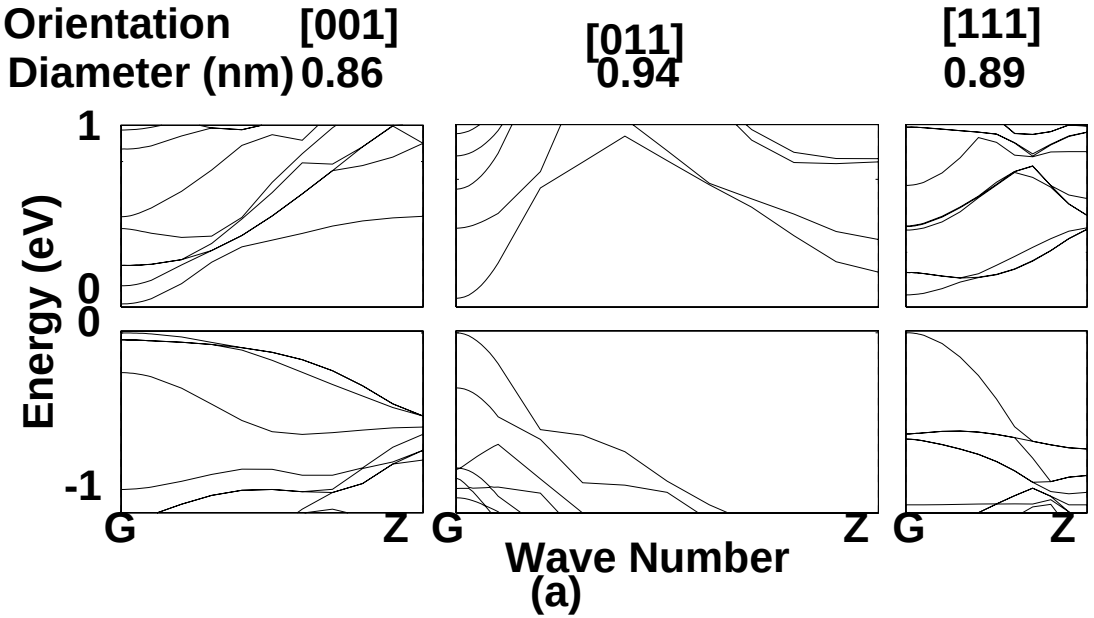


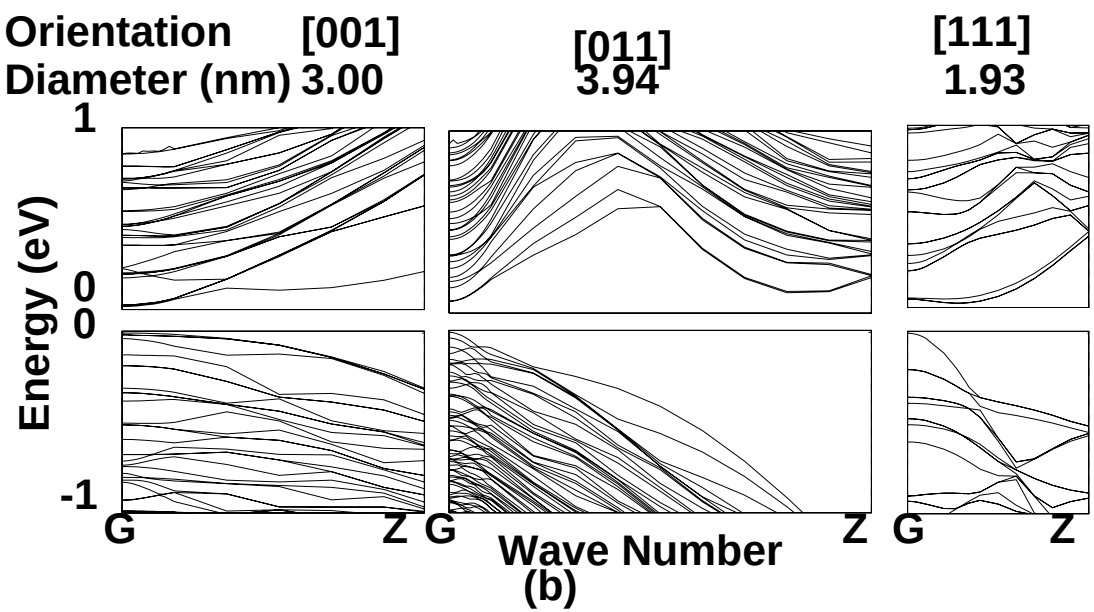
D=1.96nm
[001]

D=1.94nm
[011]

D=1.93nm
[111]

Si nanowire FET with 1D Transport





Small mass with [011]

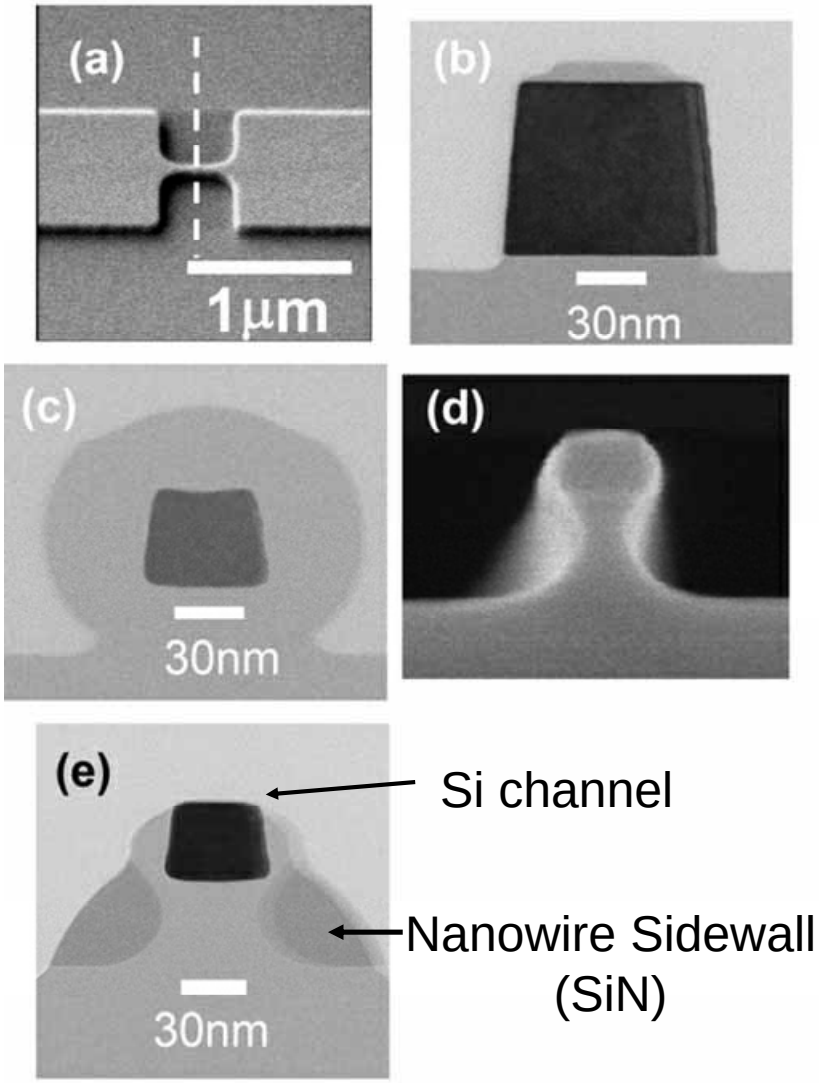
Large number of quantum channels with [001]

SiNW FET Fabrication

Brief process flow of Si Nanowire FET

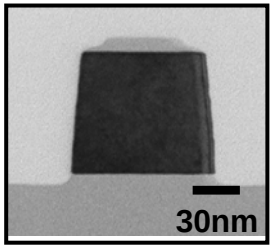
- S/D&Fin Patterining
  (ArF Lithography and RIE Etching)
- Sacrificial Oxidation & Oxide Removal
  (not completely released from BOX layer)
- Nanowire Sidewall Formation (oxide support protector)
- Gate Oxidation (5nm) & Poly-Si Deposition (75nm)
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process

(a) Fin structure formed on BOX layer. (b)XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation

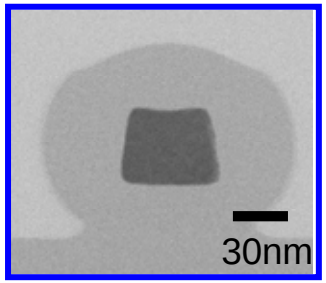


SiNW FET Fabrication

S/D & Fin Patterning

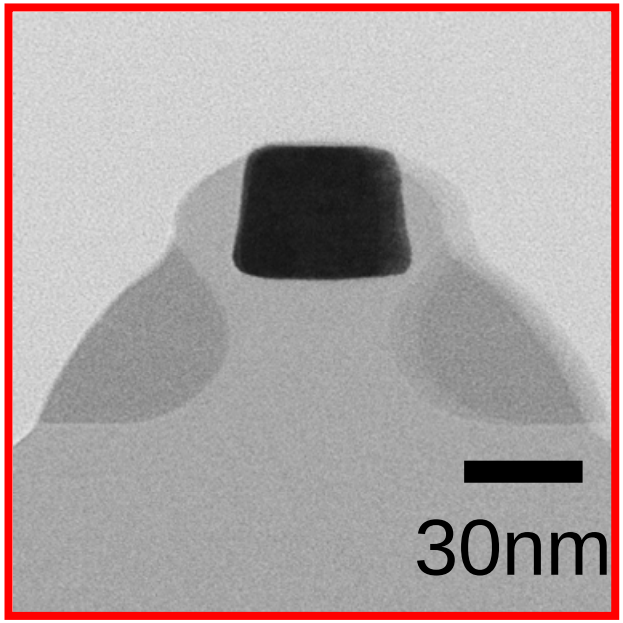


Sacrificial Oxidation



Oixde etch back

SiN sidewall support formation



Gate Oxidation & Poly-Si Deposition

Gate Lithography & RIE Etching

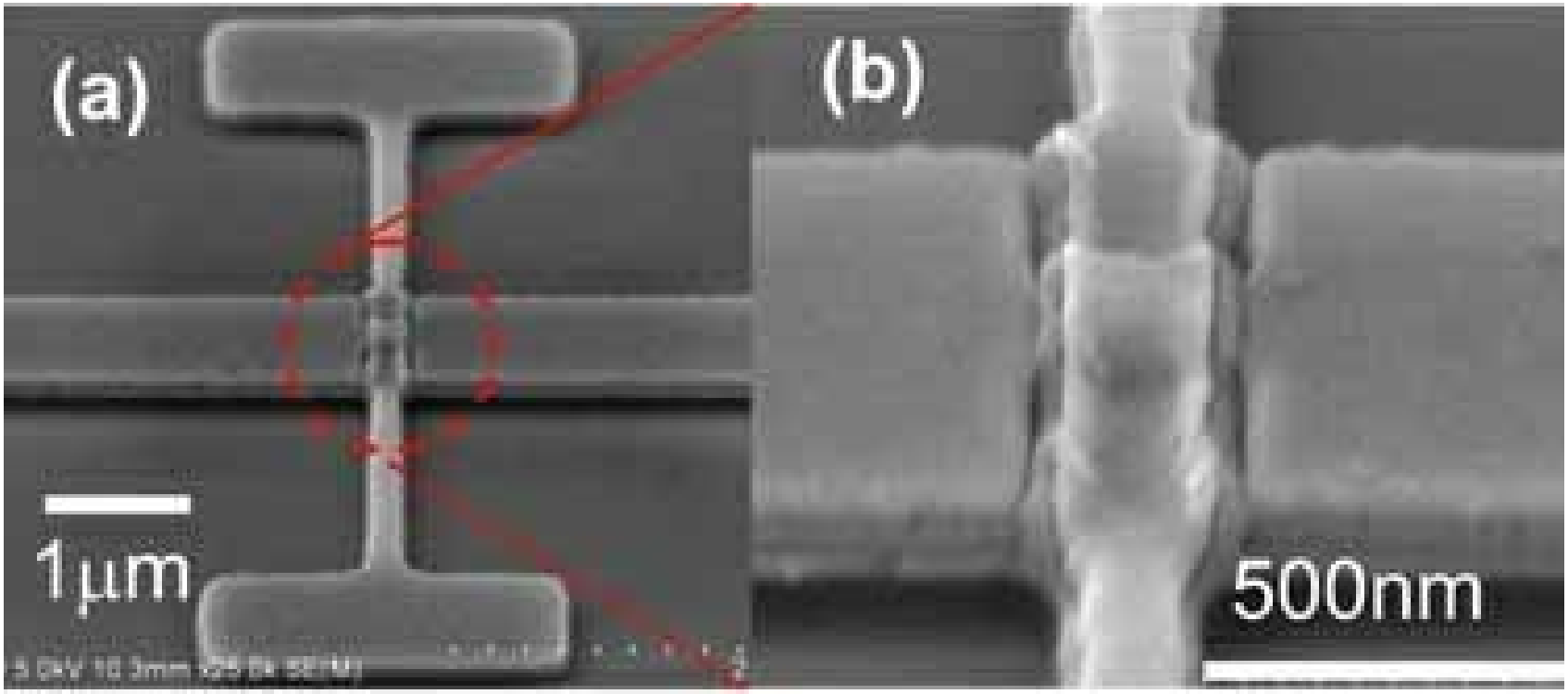
Gate Sidewall Formation

Ni SALISIDE Process (Ni 9nm / TiN 10nm)

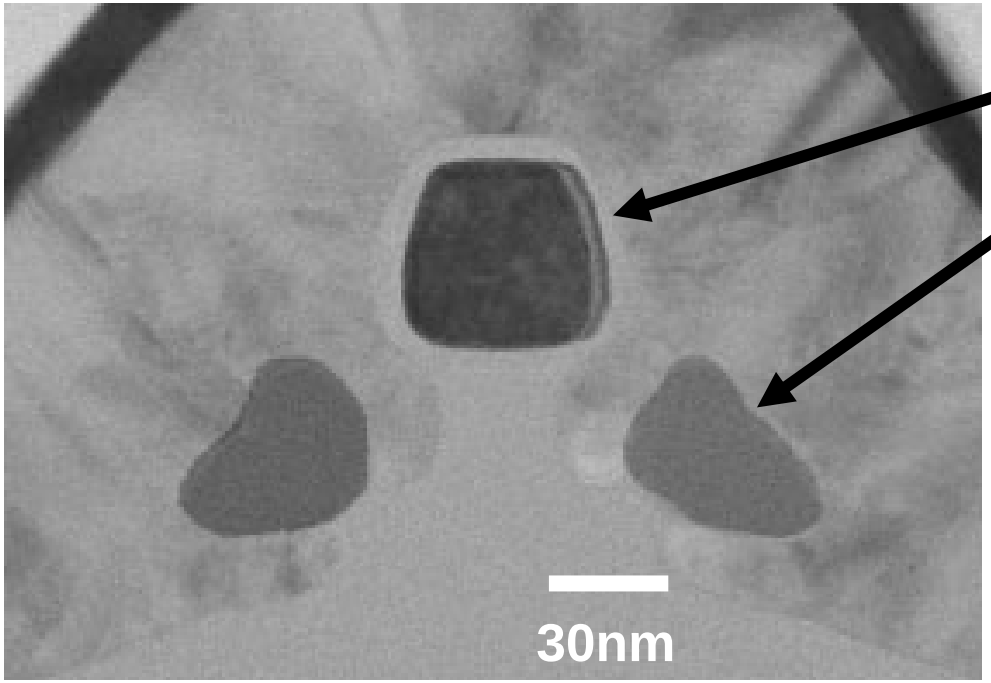
Backend

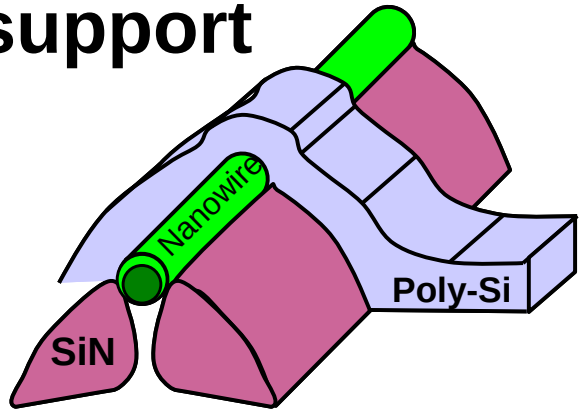
Standard recipe for gate stack formation

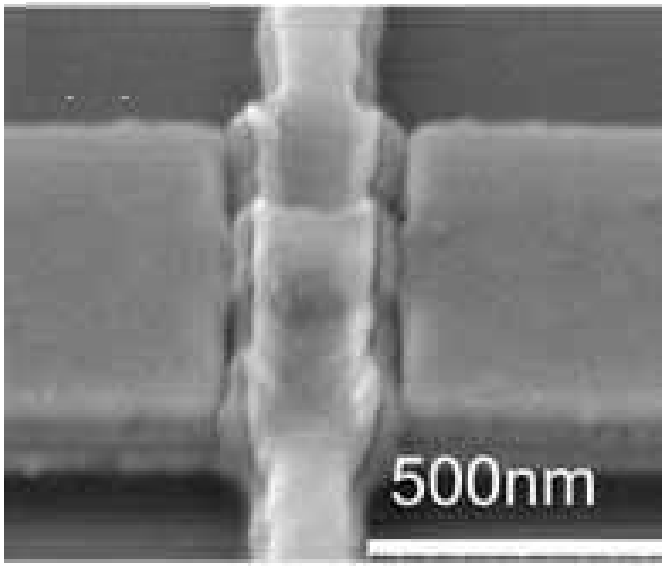
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.



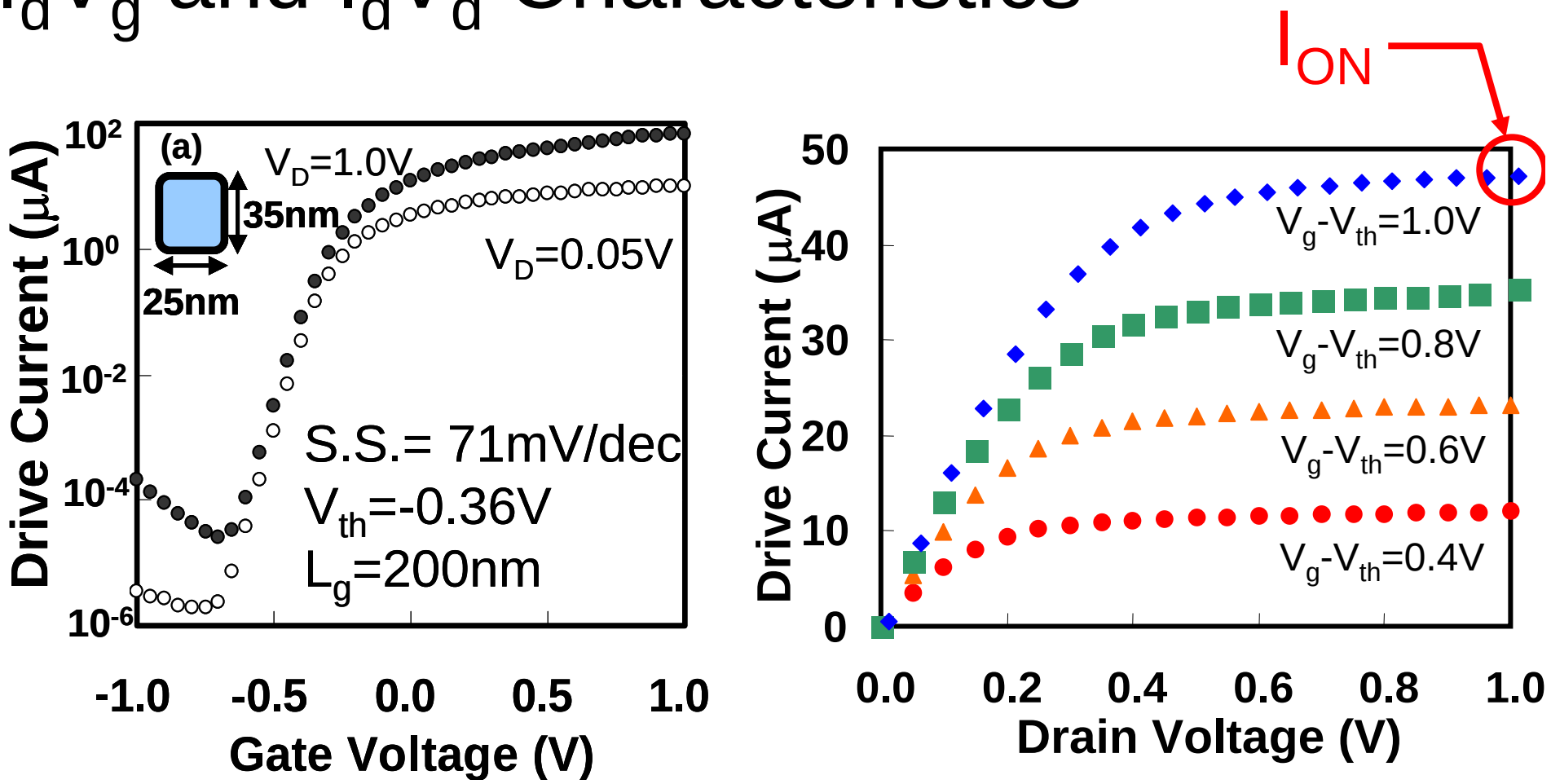
Fabricated SiNW FET





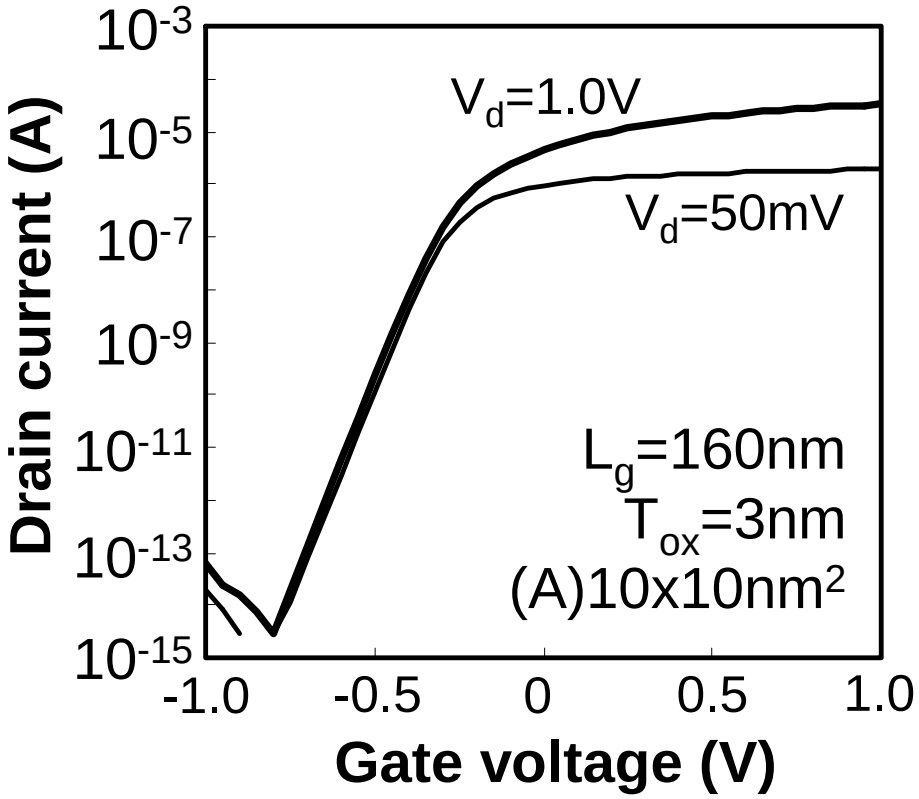


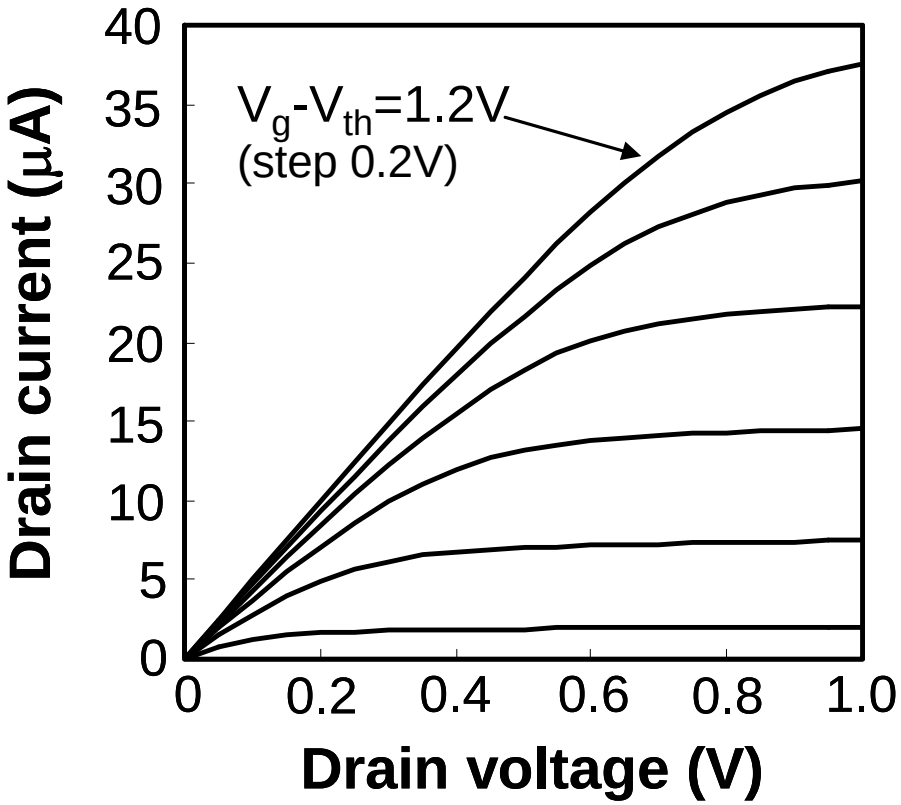
I_dV_g and I_dV_d Characteristics



I_{on}/I_{off} ratio of ~10^7, high I_{on} of 49.6 μA/wire

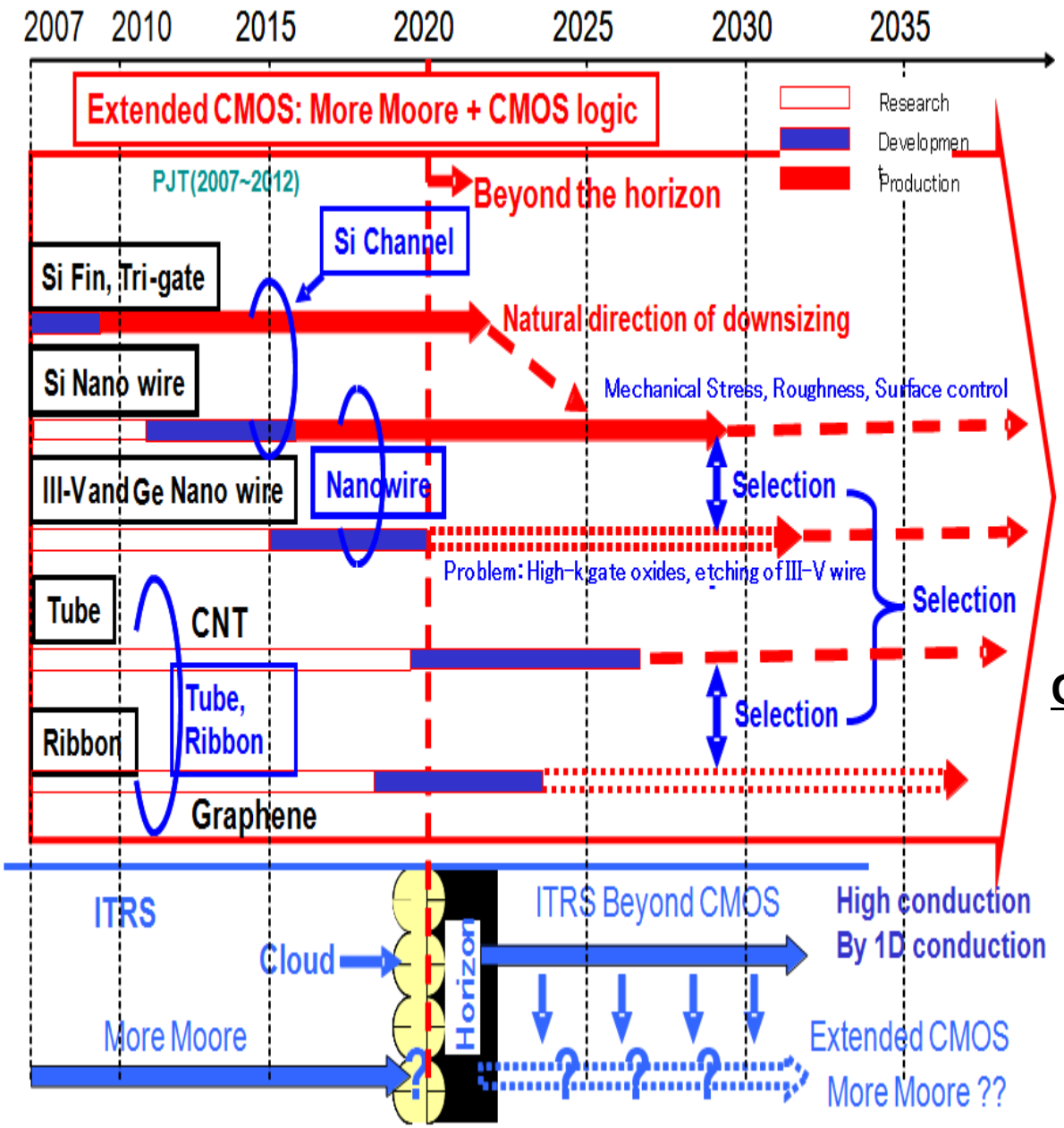
Output characteristics of 10x10cm^2 SiNW FET





Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property

Source Drain contact

Optimization of wire diameter

Compact I-V model

III-V & Ge Nanowire

High-k gate insulator

Wire formation technique

CNT:

Growth and integration of CNT

Width and Chirality control

Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique

Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

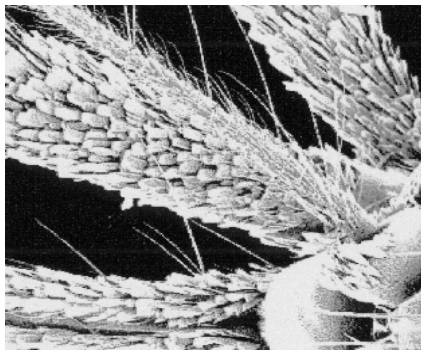
Brain

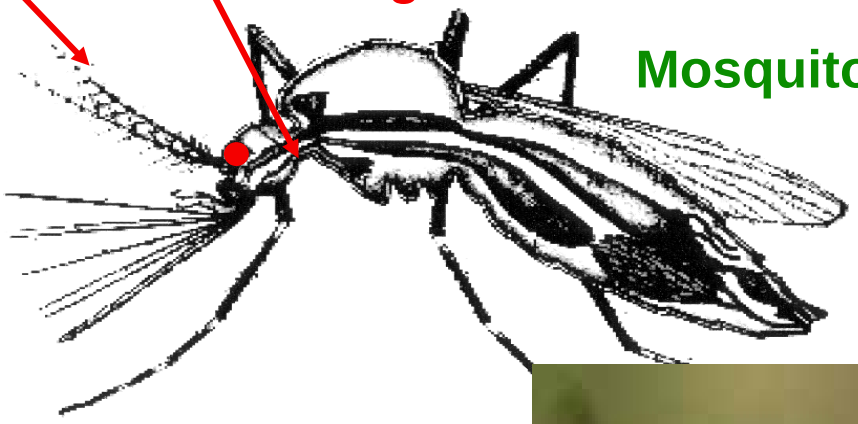
Sensor

Ultra small volume
Small number of neuron cells
Extremely low power

Infrared
Humidity
CO_2

Real time image processing
(Artificial) Intelligence
3D flight control





Mosquito

System and Algorism becomes more important !

But do not know how?

Dragonfly is further high performance

Thank you for your attgengtion